MICROELECTRONIC DEVICE INSPECTION SYSTEM IMPLEMENTATION AND MODELING FOR FLIP CHIPS AND MULTI-LAYER CERAMIC CAPACITORS

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MICROELECTRONIC DEVICE INSPECTION SYSTEM IMPLEMENTATION AND MODELING FOR FLIP CHIPS AND MULTI-LAYER CHIP CAPACITORS

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SUMMARY

Increased consumer demand for smaller electronics with more capabilities is driving the electronic packaging industry to develop smaller, more efficient component level packages. Because of this need, surface mounted components such as flip chips, ball grid arrays (BGAs), and chip-scale packages (CSPs) are being developed for use in high-volume production. Compared with traditional wire bonding packages, these packages have advantages such as a lower profile, a smaller footprint and higher solder joint density, however, these advantages come with a price. All of these technologies use solder bumps to attach the integrated circuit (IC) to the substrate instead of traditional wire lead frames. Therefore, it is difficult to search for defective connections using traditional methods such as machine vision, acoustic microscopy or x-ray inspection.

To meet this need, a novel, non-contact, non-destructive, on-line approach for inspecting solder joint quality in these packages has been developed and tested. The system consists of an Nd:YAG laser that delivers pulses of infrared energy to the surface of the chip, a laser interferometer to record surface vibrations, and a high-speed data acquisition system to record the signals. A program was written in C++ to control the data acquisition, automating the system. In this technique, the pulsed laser generates ultrasound on the chip's surface, exciting the whole chip into a vibration motion, and the interferometer measures the vibration displacement of the chip's surface at several points.

Changes in the quality of the device or its attachment to the board produce changes in the free vibration response. Using and adapting signal-processing algorithms developed for this system allows characterization of the differences between good devices and devices with defects, both in time domain and frequency domain.

Previously, this system and inspection method were used to inspect flip chips and chip scale packages for missing and misaligned solder balls, easily identifying one missing ball out of fourteen. With recent improvements to the system, the resolution for finding a damaged connection was improved. To verify these improvements, a careful study of the vibration modes excited by the laser source in a flip chip was performed, using a test vehicle that contains 48-bump flip chips with intentionally manufactured defects. The test vehicle was designed and manufactured to specification in order to achieve the best comparison between reference and defective chips. Experimental measurement of excited modes is compared with a modal analysis model created in ANSYS. A close comparison between the two sources indicates that the vibration caused by laser-generated ultrasound excites structural modal vibrations. The final goal was to establish the measurement limit for detection of open solder bumps using knowledge gained from the modal analysis to modify signal analysis algorithms. These bumps are smaller than previous bumps, and they are more closely spaced, providing a good test of the system resolution. To aid in adapting the signal analysis algorithms, the modal parameters were extracted from the experimental data, allowing for direct comparison between the data and the model.

Defects with solder bumped devices are not the only manufacturing defects that are difficult to detect during printed circuit board (PCB) assembly. Current inspection methods have been inadequate in inspecting multi-layer ceramic capacitors (MLCCs). Flex cracks in the MLCCs often cause the capacitors to fail after being cracked through flexure of the circuit board during assembly. Samples that have been cracked intentionally were compared with reference samples to determine the feasibility of using this technique to monitor the condition of MLCCs on an assembly line. Currently, there is no on-line inspection method for controlling this problem. Using the same inspection system for different types of defects in three different packages provided experimental evidence that this system can be used for a wide range of devices that have similar types of defects.

Because of the flexibility, accuracy and speed of this system, it is expected to have a great impact on the electronic packaging industry, allowing both on-line inspection, and off-line process optimization. The development of inspection techniques to identify defects in a wider range of microelectronics devices, such as more complex flip chips and MLCCs, adds to the flexibility and adaptability of the inspection system. Finite element modeling with parameterized models will aid in adapting these inspection techniques to new packages, allowing more rapid identification of modal properties that aid in inspection setup.

CHAPTER I

INTRODUCTION

Accurate, online identification of manufacturing defects present in the attachment of surface-mounted devices (SMDs) used in modern electronic assemblies is a challenging problem. Current inspection technology is expensive, time-consuming, occurs too late in the manufacturing process, or is unable to detect some common manufacturing defects. Therefore, production waste is higher than necessary, as a single bad component can mean destroying an entire assembly.

1.1 Motivation

Because of the consumer-driven need for higher-performance and smaller electronic packages, electronic manufacturing technology is struggling to meet the demand for improving manufacturing process speed and quality. One trend in electronic interconnection technology is the change from wire bonding and lead frame interconnects technology to solder bump technology. Solder bump devices and other surface mount components use small amounts of solder between the device and the printed wiring board (PWB) to connect the device. Devices such as flip chips, ball grid arrays (BGAs), chip scale packages (CSPs), and multi-layer ceramic capacitors (MLCCs) have been shown to be reliable, allowing these devices to gain rapid acceptance in electronics assembly plants

for large-scale production. Although the adoption of this technology is advantageous from the standpoint of connection speed, reduced packaging, smaller size, and lighter weight, one major drawback exists. The connections are now hidden between the device and the circuit board, so the traditional inspection methods, such as x-ray, acoustic microscopy and optical methods, have trouble finding defects in the tiny solder connections that serve as both a mechanical and electrical connection between the device and the PCB. A new on-line inspection system is needed to aid PCB manufacturers in ensuring the quality of their product in a low-cost, fast, and accurate manner. To achieve this goal, a new inspection system, based on laser ultrasound and interferometric inspection was designed, and techniques were developed to aid in accurate identification of defects in surface mounted devices.

1.2 Current Inspection Systems

In the past, there were many different ways to inspect solder joint connections between integrated circuit (IC) chips and the printed wiring board (PWB). However, with the advent of the surface-mounted technology (SMT) and solder bump technology, these methods are no longer suitable for real-time on-line inspection of solder joints (Sandra, *et al*, 1988). The following sections detail some of the past methods and discuss their shortcomings in terms of current component geometries.

1.2.1 X-Ray Imaging

One of the most popular inspection methods used in circuit board assembly is X-Ray Imaging. These systems are widely used in industrial settings, for both process development and on-line inspection (Masi, C. G., 1991). Although the method is

completely nondestructive and can detect missing solder bumps, it fails to test the actual connections of the solder joints, making it an unreliable way to verify the adhesion of the solder bump to the chips.

X-ray inspection methods work in a simple manner. High levels of radiation are passed through the board, and a detector, measuring relative changes in the strength of the radiation, samples the energy. When calibrated, this method allows measurement of small changes in material thickness, because as the x-rays pass through more material, a greater amount of radiation is absorbed (Edward, S., 1991).

However, because air does not attenuate x-rays as well as metals and solid materials, solder balls that are not adhered to the substrate appear the same as properly connected solder balls (Wright, 2001). The small air gap caused by a non-wet ball, visible under a microscope, is not sufficient to cause a large change in the strength of the x-rays, but it is enough to cause a malfunction in the operation of the chip. In addition, the x-ray images are pictures that require some interpretation, such as a machine vision application that scans the image of each bump. This can be time-consuming and expensive to implement. Because of these limitations, this method is not well-suited for online solder bump inspection.

1.2.2 Scanning Acoustic Microscopy

Another widely used method is scanning acoustic microscopy (SAM). The method relies on ultrasonic propagation through material and the corresponding changes in either the transmitted or reflected signals through materials or interfaces (Adams, T.,

1995, 2000). Several commercial systems are available from suppliers such as Sonoscan Incorporated.

For these systems, the samples are immersed in a tank of liquid. Although alcohol or other liquids can be used, water is the most common. Using the liquid as an efficient coupling medium, high frequency ultrasound, 10 MHz and above, is propagated through the specimen. The ultrasonic pulse enters the specimen, interacts with the chip and solder bumps, and a receiver picks up either the portion of the pulse that is transmitted through the specimen, or the portion that is reflected from the bottom of the chip. Because the solder material transmits the energy very well, a properly adhered bump will have high transmission of the wave. Therefore the reflected signal will be lower. The ultrasonic pulse can be focused to a very small spot on the interface being monitored, and waveforms are recorded as the ultrasonic system performs a raster scan over the specimen. Changes in the signal are translated to a color in order to create an image of the specimen. Defects such as pre-exisiting voids, cracks, or non-wet solder joints can be located using this technique (Semmens, J. E., *et al*, 1997).

Although ultrasonic techniques are powerful, there are some specific limitations that prevent it being used for solder joint inspection. It is unsuitable for on-line inspection because most electronic components cannot be immersed in water without detrimental effects, and many of the other solvents raise safety issues with the machine operators. In addition, the raster scanning takes some time, approximately five minutes or more, which could slow down a manufacturing line. Because many solder balls are placed near the edge of a specimen, they are difficult to see with this technique (Kubota,

J., *et al*, 1992). Reflections of the propagating wave blur the actual image of the solder joints near the edge. As solder joints continue to decrease in size, the frequency of ultrasound will have to be increased to maintain adequate resolution of the solder balls. Unfortunately, as frequency increases the amount of attenuation also increases, making it very difficult to propagate a high frequency signal through twice the thickness of an SMT device.

1.2.3 Other Methods

There are several other methods that have been used to detect solder joint defects in the past. However, these also have limitations that prevent them from being used for new solder bumped chips. These limitations are based on changes in geometry of new packages or the increasing complexity of the electronic packages.

Solder lead vibrometry was used to inspect the leads on some SMTs while wire leads were still used to connect them to the board (Lau, J. *et al*, 1989). Using this method, a jet of air was directed at the wire leads, and any leads that were unconnected were detected through changes in the vibration frequency. However, with the move to solder bumps, an air jet cannot be used to excite the bumps into motion.

Machine vision techniques have been used to inspect solder joints as well (Sandra, L. B. *et al*, 1988). Techniques were developed to detect the shape of a solder joint and correlate that with some measure of solder joint quality. Although machine vision is used to inspect the size, shape, and placement of solder bumps before the chips are placed over them, this method is also unsuitable for the solder bump inspection since cameras cannot see through either the substrate or the chips.

Currently, many manufacturers use electronic methods, such as the flying probe or bed of nails techniques (Newman, K.E. *et al*, 1998). These techniques use changes in electrical resistance and impedance to detect poorly bonded chips. Probes reach down from above the board and touch inspection points. Then small electrical impulses are passed through the chips to check each joint. Although these techniques do test the functionality of the active or passive component and their interconnects, joints that have poor bonds or are simply making mechanical contact with the surface of the chip are not detected. In addition, these methods are time-consuming and expensive to implement, and they will become even more so as the industry continues to make more complex chips.

Therefore, the system under development will be a valuable new tool for manufacturing inspection because the system fills in the inadequacies of the other systems. The system is non-destructive, fast, accurate, flexible for many devices, and it can detect small air gaps. Further development of this system will lead to even more applications, as the structural properties of a system can cause a significant change in the system's impulse vibration response.

1.3 Project Objective

The scope of this research is to continue development and test an automated system for solder joint quality measurements that will be flexible enough to meet present and future demands in the electronics packaging industry. Although the system is currently unable to be used on-line, it serves as a laboratory test-bed for developing new signal analysis techniques. The final goal of this research is to develop a machine that

will fit directly into an industrial assembly line. By making the laboratory setup flexible, a wide variety of chips may be tested in the future with minimal changes in holding fixtures.

A novel solder-joint inspection system has been developed based on laser ultrasound and interferometric techniques (Monchalin, J. P., 1989). A pulsed laser generates ultrasound on the chip's surface and the whole chip is excited into vibration modes. An interferometer is used to measure the vibration displacement of the chip's surface at several points, and solder joints with different qualities cause different vibration responses (Lau, J. *et al*, 1989). In addition, this method is sensitive to defects on the surface of the chip, such as cracks, chip, or gross misalignment (Howard, et.al., 2002), (Liu, et.al, 2000) .

The interferometric system used provides an alternative to traditional solder-joint inspection methods. Detection of defects does not depend on inspecting each solder joint individually, so the technique can be made to operate very quickly. A missing solder ball causes an effect in a larger area, not just at the location of the missing ball. A change in the constraint on the system affects the mode shape and the vibration signature that is recorded by the interferometer. Since the chips do not have to be inspected at every point, the method is fast and can be used for inspection of solder joint quality on-line during manufacturing and off-line during process development.

Unfortunately, there is a limitation to the process. To understand how the signal will change as a result of a defect, knowledge about how the defect affects the response must be known. Vibration responses from known chips with good connections and

known types of defects must be found for comparison. Therefore, the initial set up and training of the system may require some effort, especially in the production of defective samples.

Because each new type of sample requires extensive testing to determine the changes in vibration response, an systematic approach, based on structural modal analysis is presented. This approach uses the modal vibration properties of a system to more rapidly and more accurately determine the changes that are measured between the vibration response of good and defective specimens. Modal properties are determined through signal analysis methods, and they are verified using a finite element model.

As a result, the sensitivity of the inspection system to open solder bumps between a flip chip and the circuit board is determined. In addition, the sensitivity of the inspection system to flex cracks in multi-layer ceramic capacitors is determined. These two packages represent more difficult inspections than have previously been performed, but a modal analysis approach helps to simplify the process of finding the subtle changes in vibration response that are observed experimentally.

The rest of the document describes in detail the equipment setup and characterization, the creation of flip chip and MLCC test vehicles, signal analysis and defect identification for both packages, modal parameter extraction and analysis for the flip chip samples, and finite element modeling of the modal behavior of the flip chip package. Chapter II contains a summary of the current knowledge in the following areas: SMT assembly and common manufacturing defects, methods used to find manufacturing defects, laser ultrasonic generation, modal parameter extraction and modal finite element

analysis. In addition, the chapter provides an explanation of previous work relating to the laser vibration analysis method. The equipment used in constructing the system is described in Chapter III, along with an overview of the data acquisition and processing software. Chapter IV contains the experimental procedure, error analysis, sensitivity analysis and an overview of the data collection and analysis software used. The results from the flip chip case study on the 48-ball, daisy chain test die are presented in Chapter V, and this chapter presents the basic inspection into the vibration behavior of the flip chip package. Chapter VI presents the Error Ratio (ER) analysis and measurement limit determination for the system used to detect open solder bumps under a flip chip package. Chapter VII contains the modal parameter extraction and analysis, showing that the measurement limit of the technique is approximately the same for both methods. Chapter VIII presents the finite element modeling and analysis performed to capture the modal vibration parameters for the flip chip test die. All of the results from three MLCC samples are presented in Chapter IX, along with the associated signal analysis routines. Conclusions drawn from the results and their impact are covered in Chapter X, and a summary of the most significant contributions of this work is presented in Chapter XI, followed by some suggestions for future research in Chapter XII.

CHAPTER II

LITERATURE REVIEW

Although a wealth of knowledge exists regarding the manufacture and assembly of surface-mounted devices (SMTs) and the detection of manufacturing defects in these devices, the early identification of defects, which could lead to cost savings by reducing waste, remains a difficult problem. An understanding of the current manufacturing processes and potential defects is necessary to identify defects that can be detected and repaired before the product is completely assembled. In spite of the efforts to control and detect manufacturing defects online, none of the current systems are suitable to identify these defects. Therefore, a unique approach, borrowing from the field of structural modal analysis is applied to the microscopic structures of SMT devices. This chapter first provides an overview of the manufacturing processes for flip chips, identification of common manufacturing-related defects, and current defect identification methods. An overview of the manufacturing processes, common defects and current identification methods are also provided for MLCC packages. Finally, a summary of the potential modal analysis approaches for structural defect detection in packages is presented, including the finite element analysis approach for extracting modal parameters.

2.1 Flip Chip Processing

In developing any new kind of technology it is important to understand where it will fit in with, improve or revolutionize existing technology. The solder joint inspection system used in this work was developed in the course of previous work by Erdahl, et.al. (2000), Liu, et.al. (2001) and Howard et.al. (2002). The system is designed to fit into a specific place in the flip chip attachment process during circuit board manufacturing. A brief description of the initial stages of solder-bumped chip attachment provides a clearer idea of how this system will merge with the existing technology. Flip chip solder joint connections with a circuit board, such as those shown in the upper right of Figure 2-1, are being inspected in the course of this discussion. However, other solder-bumped devices, such as chip scale packages (CSPs), ball grid arrays (BGAs), and multi-chip modules (MCMs) follow a similar attachment and inspection procedure.

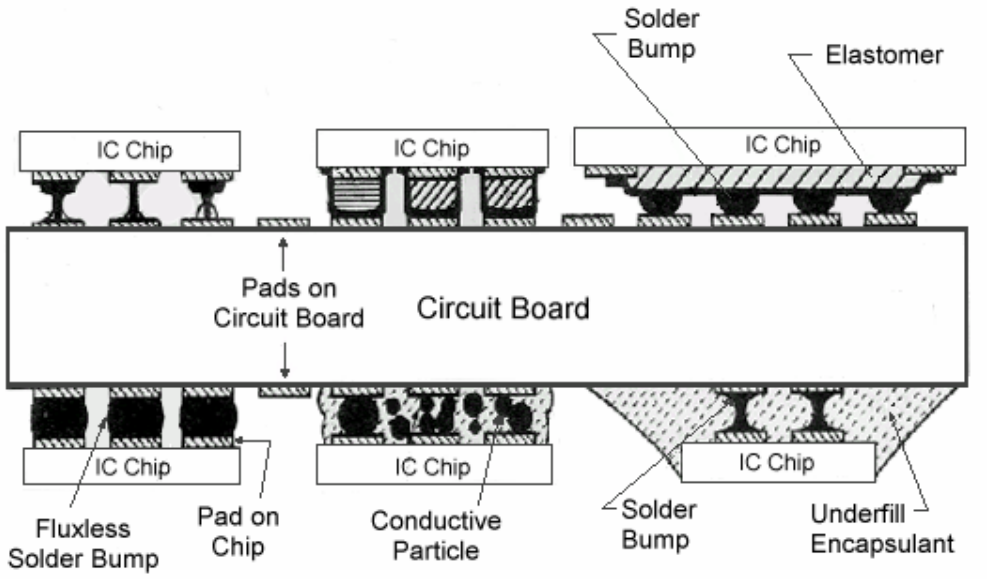


Figure 2-1: Surface Mounted Devices

As with any solder bumped technology, the flip chip attachment process begins with placing the flip chip on the board. Before placing the chip, a solder paste is sometimes deposited using either a screen-printing process or a small syringe in order to cover the solder joint attachment pads on the printed wiring board. Paste is deposited to help the chip adhere to the board and to hold the chip in place during solder reflow, a heating process that melts the solder and creates the bond between the chip and the board. The solder balls are attached to the underside of the chip before placement on the board. After this, other types of sensors often scan to make sure that all of the solder pads on the board have been properly and evenly covered with solder paste (Blackwell, 2000).

In the next stage, a pick-and-place machine is used to accurately place the chips on top of the solder balls. Positioning is extremely accurate, and the machines can place thousands of chips per hour (Blackwell, 2000). A camera is used to find the exact location referenced to fiducial marks on the corners of the board. If placement tolerances are extremely small for a specific component, then fiducials close to the chip location are used to correct the final location of the chip, after the additional fiducials are found based on the initial measurement. An automated CCD camera is used to inspect the underside of the chip to ensure that all of the solder bumps are present. To clean all of the contacts, and to help hold the chip in place, the chip is dipped into a thin layer of flux before setting the chip down on the board. The flux helps the wetting process, and it is very important to use for cleaning the contacts before the final solder joints are created.

At this point, the entire assembly is passed through a reflow oven. The oven brings the entire assembly above the liquidus temperature for the solder in use, and the

solder reflows, wetting the surface of the chip and the surface of the substrate (Blackwell, 2000). Special care is taken to create under bump metallurgy (UBM) that keeps the solder in small cups, and the UBM material is designed to allow proper wetting between the solder and the chip. The UBM helps prevent solder shorts and encourages good bonds between the chip and substrate, and the surface tension of molten solder helps align the chip to the solder pads.

After leaving the oven, the chips should be solidly attached to the circuit board. However, sometimes the solder balls do not wet the UBM on the chip, or the balls are not attached to the circuit board correctly. It is at this point that missing solder balls or other defects if found could be potentially corrected. This is the point where an efficient inspection machine fits into the manufacturing process. For the technique chosen in this research, it is important that the solder joints be inspected before the underfill is added to the package.

The underfill process finalizes the chip attachment procedure, and once completed, no reworking can be performed. Underfill is a low-viscosity epoxy that completely fills the volume around the solder bumps and between the die and the board. After curing, the underfill serves to strengthen both the mechanical attachment of the die to the board and to provide a strain-relief mechanism that helps match the coefficient of thermal expansion between the silicon die and the board.

2.2 Flip Chip Inspection Methods

Flip chips have multiple failure modes, which can be within the structure of the chip, the connection of the chip to the solder bumps, or the connection of the solder

bumps to the board (Semmens and Adams, 1998). Because flip chips are an "active" part of any circuit and because they are one of the more expensive components, a wide array of inspection techniques have been used to help detect failures and determine the cause of failures. Some of the failures, if caught before the final manufacturing steps, can be repaired, reworked, or the part can be replaced, preventing the entire circuit board assembly from becoming manufacturing scrap. An overview of the inspection techniques that have been applied to detecting failures in flip chips is presented. However, special attention is given to techniques that can be applied within the manufacturing process.

2.2.1 Failure Analysis

Although the focus of failure analysis is on the determination of the exact nature of failure, instead of screening for defects during manufacturing, the basic concepts of imaging and defect identification are the same. An overview of the failure analysis methods used to find defects in flip chips provides a roadmap of the following discussion. When looking for applicable techniques to apply during manufacturing, the natural way to start is to examine the techniques used to identify problems with chips that have reached consumers and proven to be problematic. The field of failure analysis techniques applied to integrated circuit (IC) devices is clearly summarized and categorized by Soden, et. al. (1997), and the methods are broken down into the following categories:

- Electrical measurement and testing (flying probe, functional, etc.)
- Physical (destructive cross-section and peel-off)
- Indirect and Nondestructive methods

Electrical measurements and performance testing are used in industry to check boards before they are shipped to consumers. However, some types of defects can be missed by these methods. The variety of techniques developed to inspect flip chips is a testament to their importance to future manufacturing. Destructive physical analysis is always an option to investigate reasons for proven failure, but it cannot be used as a screening method. Therefore, the other indirect and nondestructive techniques are more useful for the scope of this investigation. Some of the popular methods are listed below:

- Thermal Imaging
- Optical Methods (microscopy, endoscopy, machine vision, etc.)
- Electron Beam
- Ion Beam
- Scanning Probe (x-ray, acoustic microscopy, SQUID microscopy, etc.)

The following subsections describe these methods, their applications, and their shortcomings for online inspection.

2.2.2 Flip Chip – Electrical and Functional Tests

Currently, many manufacturers use electronic methods, such as the flying probe or bed of nails techniques (Newman, K.E. *et al*, 1998). These techniques use changes in electrical resistance and impedance to detect poorly bonded chips. Probes reach down from above the board and touch inspection points. Then small electrical impulses are passed through the chips to check each joint. Although these techniques do test the functionality of the active or passive component and their interconnects, joints that have

poor bonds or are simply making mechanical contact with the surface of the chip are not detected. In addition, these methods are time-consuming and expensive to implement, and they will become even more so as the industry continues to make more complex chips.

2.2.3 Flip Chip – Machine Vision

Machine vision techniques have been used to inspect solder joints as well (Sandra, L. B. *et al*, 1988). Techniques were developed to detect the shape of a solder joint and correlate that with some measure of solder joint quality. Although machine vision is used to inspect the size, shape, and placement of solder bumps before the chips are placed over them, this method is also unsuitable for the solder bump inspection since cameras cannot see through either the substrate or the chips.

2.2.4 Flip Chip – Backside Infrared Imaging

Backside infrared imaging relies on the fact that the P-N junctions within the chip emit energy as they are activated and deactivated. Probes and techniques are used to detect changes to the emission spectra, indicating a change in performance. The techniques can be classified into two approaches: passive and active (Barton, et.al., 1999). Both approaches watch for emission spectra changes, but the active approach provides an additional stimulus to increase the ability of the sensors to detect a change.

Passive techniques include photon emission spectroscopy (PEM) and picosecond integrated circuit analysis (PICA) (Barton, et.al., 1999). These techniques measure light emissions from the P-N junctions of a sample during operation, but they do not excite the

specimen. The intensity and the frequency of electrical transients within the die can be monitored during operation of the chip, and ambient light emissions are recorded (Tsang and Kash, 1996). Changes in the emission spectrum, the intensity of the detected pulses, or the frequency of the detected pulses indicate changes in chip's performance.

If a probe, such as an electron beam, ion beam or a photon beam, is used to interact with the specimen, then the technique is considered active (Barton, et.al., 1999), (Singer, 1996). Several active techniques have been developed: Laser Voltage Probe (LVP), scanning optical microscopy techniques, LIVA (Light-Induced Voltage Alteration), and TIVA (Thermally-Induced Voltage Alteration). All of these techniques use a stimulation technique to cause a measurable change in voltage for a properly working IC chip. The voltage change is monitored, and the resulting values are scaled to performance of the device.

The main drawback for the entire complement of backside imaging techniques is clear. In order for the light emission to be detected, the die must be "thinned" before measurements can be taken, requiring a milling or ion-beam process to take the silicon die (chip) from 650 μm thick to 100-150 μm thick (Chiang, Part II 1999), (Barton, et.al, 1999), (Chiang and Hurley, 1998). Since the thinning process is time-consuming and weakens the die structure, this class of inspection techniques is unsuitable for application to a manufacturing environment, where the thickness of the chip contributes to the overall reliability of the package (Chiang, Part I, 1999). These techniques are well-suited for finding out reasons for poor performance after failure has occurred in the field, but they are unsuitable for a screening process.

2.2.5 Flip Chip – Endoscopy (Optical)

Falling under the category of optical techniques, endoscopy is commonly applied in the medical field to look inside internal organs. An endoscope, a side-viewing microscope on a small flexible probe, is used to visually inspect underneath flip chips, CSPs, and BGAs to determine standoff height, detect cold joints, identify poor contact, view cracks, and inspect inner rows of bumps (Chan, Tang, and Tu, 2000) (Zweig, 2002). Although systems are commercially available, the inspection process requires a human to view the images and perform the inspections. Therefore, the throughput and accuracy may not be suitable for manufacturing (Zweig, 2002). In addition, because the inner rows of bumps are not fully visible, only gross anomalies can be detected, such as warping of the PCB or component, evidence of flux residue or the general surface appearance of the interior bumps (Chan, Tang, and Tu, 2000). Without intelligent software to automatically inspect for defects, use of an endoscope for manufacturing will not be an adequate solution for online use.

2.2.6 Flip Chip – SQUID Microscopy

Another method that has been applied to imaging internal defects with flip chips is the application of a superconducting quantum interference device (SQUID), a sensitive magnetic sensor (Knauss, et.al., 2001). An advantage to this technique is the low frequency magnetic waves that easily penetrate the IC package, allowing observation of the magnetic fields created by propagating current in the device. The main disadvantage remains the problem of application, as the SQUID coil must be cooled to cryogenic temperatures in order to accurately measure small magnetic field changes (Fleet, et.al.,

1999). Images are created by taking magnetic field measurements in a raster scan over the surface, which removes any DC magnetic field and allows mapping of small changes within the device (Knauss, et.al, 2001). This method is primarily used in defect identification after detection through an electrical test, however, commonly identified defects include the following: shorts within the IC chip, shorted joints, and open joints. Changes in desired path of electrical current that indicate defects are detectable, however, the technique is not practical for manufacturing screening tests because of the complexity of the equipment.

2.2.7 Flip Chip – X-Ray

Although the previously mentioned alternative systems are primarily applicable to offline failure analysis instead of screening, x-ray systems have progressed to the point of automated online inspection. Remaining one of the most popular inspection methods used in circuit board assembly, both Automated X-Ray Imaging (AXI) and non-automated systems provide a fast and intuitive means of inspecting the interior of the flip chip assembly. These systems are widely used in industrial settings, for both process development and on-line inspection (Masi, C. G., 1991). Although the method is completely nondestructive and can detect missing solder bumps, it fails to test the actual connections of the solder joints, making it an unreliable way to verify the adhesion of the solder bump to the chips.

Basic x-ray inspection methods are easy to explain, and the simplicity of the process is both its strength and weakness. High levels of radiation are passed through the board, and a detector, measuring relative changes in the strength of the radiation, samples

the energy. When calibrated, this method allows measurement of small changes in material thickness, because as the x-rays pass through more material, a greater amount of radiation is absorbed (Edward, S., 1991). Small changes in material thickness or changes in material type can be easily detected. Spatial resolution is only limited by the sensitivity of the detection method, allowing internal views of specimens that look like they are being taken through a microscope.

Although the x-ray images are impressive, the x-ray images are pictures that require some interpretation, such as a machine vision application that scans the image of each bump, a time-consuming and potentially subjective process (Zwieg, 2002). To alleviate the subjective process, Zwieg also proposed a solder bump signature method that monitors the overall shape of bumps to infer the presence of: deformation failures such as doming or dishing, misalignment, excessive or missing solder paste, PCB construction problems and bond area errors (2002). This method could be used to automate the image processing, however, as implemented, endoscopy is used to verify, check and properly identify failures, making this method unsuitable for online inspection. In addition, because air does not attenuate x-rays as well as metals and solid materials, solder balls that are not adhered to the substrate appear the same as properly connected solder balls (Wright, 2001). The small air gap caused by a non-wet ball, visible under an optical microscope, is not sufficient to cause a large change in the strength of the x-rays, but it is enough to cause a malfunction in the operation of the chip.

To overcome the problem of low air-gap attenuation, both oblique viewing and 3D x-ray inspection systems have been implemented (Lehmann, 2002). By rotating the

sample or taking a 3D image, the profile of solder bumps attached to the board can be examined and changes in the profile indicate connection problems such as open joints or wetting failures occur can be detected. However, both oblique and 3D methods are slower than traditional 2D x-ray systems, so they are still not practical for online inspection. The entire process of image processing and visual inspection of x-ray images can be time-consuming and expensive to implement. In addition, even with the added capability of these systems, some of the solder bumps are difficult to view in relation to neighboring features on a circuit board. Because of these limitations, this method is not well-suited for online solder bump inspection.

2.2.8 Flip Chip – Ultrasound and Acoustic Microscopy

To overcome the problem of small attenuation changes for air gaps seen in x-ray systems, ultrasonic techniques have been employed. These systems use propagating ultrasonic bursts, which are reflected by the solid-air interface and are used to find internal delaminations, cracks, inclusions, and to measure the thickness of materials. More than one technique can be employed to find a specific type of defect, and contact transducers are used in conjunction with immersion transducers for detecting different defects in the same devices (Abdul, *et. al.*, 2003). However, ultrasonic imaging has some drawbacks that prevent the technique from being the preferred method for online inspection.

The most direct ultrasonic imaging method for monitoring the interfaces between solder connections and the component or board is scanning acoustic microscopy (SAM). The method relies on ultrasonic propagation through material and the corresponding

changes in either the transmitted or reflected signals through materials or interfaces (Adams, T., 1995, 2000). Raster scans of the whole specimen are necessary, and time gates are used on the propagating signal to allow for monitoring of a pre-set depth of material. Many commercial systems are available from suppliers such as Sonoscan Incorporated, Sonix, and Panametrics, and the method has been effectively applied to packages such as flip chips, BGAs, internal defects in plastic lead frame IC components, and in multi-chip modules (MCMs) (Harsanyi, et.al., 2000).

For these systems to work effectively, the samples are immersed in a tank of liquid. Although alcohol or other liquids can be used, water is the most common. Using the liquid as an efficient coupling medium, high frequency ultrasound, 10 MHz and above (up to 300 MHz), is propagated through the specimen (Semmens and Kessler, 2002). The ultrasonic pulse enters the specimen, and the acoustic energy interacts with the chip and solder bumps. Interfaces and defects scatter ultrasonic energy, and a receiver picks up either the portion of the pulse that is transmitted through the specimen, or the portion that is reflected from an interface. Some common interfaces are the following: the bottom of the chip/bump interface, the chip/underfill interface, the bump/board interface, the underfill/board interface or any interface between an internal voids or crack and the material (Lawton and Barrett, 1996). Because the solder material transmits the energy very well, a properly adhered bump will have high transmission of the wave. The ultrasonic pulse can be focused to a very small spot on the interface being monitored, even if it is within the material, and waveforms are recorded as the ultrasonic system performs a raster scan over the specimen. Changes in the amplitude of the signal within a small time gate are used to capture the response from a single interface. This

amplitude is translated into a color in order to create an image of the specimen. Defects such as pre-existing solder bump voids, cracks in the bumps or the die, undersized and bridged bumps, underfill voids and delaminations, or non-wet solder joints can be located using this technique (Slattery, et.al., 1995), (Semmens, J. E., *et al*, 1997), (Semmens and Adams, 1998). Higher propagation frequencies have greater resolution for small changes in material properties caused by internal defects, but a trade-off exists between resolution and penetration depth as higher frequencies attenuate faster within a material (Lawton and Barrett, 1996).

Instead of examining just the amplitude of the reflected ultrasonic energy, frequency methods can be utilized to analyze the entire collected waveform to show additional information about the interior condition of the specimens (Semmens and Kessler, 2002). Breaking the recorded pulse into small bands in the frequency domain to produce frequency domain images has been shown to provide additional details about the internal structure that were not visible on the time domain images (Semmens and Kessler, 2002).

Ultrasonic methods have also been used to screen for qualities that indicate future reliability problems. Acoustic microscopy was used to measure the standoff height of flip chips on flexible substrates (Tang, et.al., 2000, 2001). A 230 MHz transducer was used to measure the time-of-flight through the chip to the surface of the flex substrate in order to ensure proper bonding. If the height is inaccurate, solder joints are misshapen and inadequate underfill will lead to early failure (Tang, et.al., 2001).

Another application of scanning acoustic microscopy has been to check for delaminations between flip chips and the underfill layer (Hutt, et.al., 2000). For monitoring the adhesion of the underfill to the die and to the substrate, a 230 MHz transducer was used, and the reflected echoes from the interfaces were collected in a raster scan to create an image of the interface, since near total reflection of the sound occurs at the air or vacuum interface present when a delamination occurs. However, sometimes, the delamination was undetectable although the entire die was not adhered to the underfill (Hutt, et.al., 2000).

Contact transducers have been used to monitor the Silicon/Copper interfaces for die attach devices (Abdul, et.al., 2003). Adhesive is used to directly attach the silicon die to a copper substrate, and the contact transducers, at 2.5 and 7.5 MHz, provide a means of evaluating the interface. C-scan images and reflection coefficients were used to measure degradation of the interface when it was exposed to moisture to weaken the bond. The technique was effective, but contact transducers cannot be used for an online manufacturing system.

Although ultrasonic techniques are powerful, there are some specific limitations that prevent it being used for online solder joint inspection. It is unsuitable for online inspection because most electronic components cannot be immersed in water without detrimental effects, and many of the other solvents raise safety issues with the machine operators. In addition, the raster scanning takes some time, which could slow down a manufacturing line. At best, ultrasonic systems are capable of scanning only a few hundred parts in an hour, and this limits the application of this method to screening and

sampling applications (Adams, 1996). However, a properly designed automated system can reach nearly the speed necessary for online operation through handling trays of parts at a time, but the system is much more complex than the standard system (Adams, 1996). Unfortunately, the requirement of a liquid couplant means that every part must be immersed, and then cleaned and/or dried before continuing with the final manufacturing processes, adding several more stages and even more equipment to the manufacturing line.

Because many solder balls are placed near the edge of a specimen, they are difficult to see with this technique (Kubota, J., *et al*, 1992). Reflections of the propagating wave blur the actual image of the solder joints near the edge. An attempt to mitigate this problem was made by Semmens (2000) with a specially modified transducer that corrects for some edge effects. As solder joints decrease in size, the frequency of ultrasound will have to be increased to maintain adequate resolution of the solder balls. Unfortunately, as frequency increases the amount of attenuation also increases, making it very difficult to propagate a high frequency signal through twice the thickness of an SMT device. Eventually a limit will be reached, as silicon die cannot get much thinner without reducing reliability.

2.2.9 Flip Chip – Solder Lead Vibrometry

Solder lead vibrometry was used to inspect the leads on some SMTs while wire leads were still used to connect them to the board (Lau, J. *et al*, 1989). Using this method, a jet of air was directed at the wire leads, and any leads that were unconnected

were detected through changes in the vibration frequency. However, with the move to solder bumps, an air jet cannot be used to excite the bumps into motion.

Therefore, the system under development will be a valuable new tool for flip chip manufacturing inspection because the system fills in the inadequacies of the other systems. The system is non-destructive, fast, accurate, and flexible for many devices, and it can detect small air gaps. Further development of this system will lead to even more applications, as the structural properties of a system can cause a significant change in the system's impulse vibration response.

2.3 MLCC Device Overview

Multi-layer Ceramic Capacitors (MLCCs) are one of the most prolific surface mounted devices used in commercial applications today. Originally developed in the 1970s, these devices have found applications in every field, and they are contributing to the rapid decrease in size (down to 0.001" by 0.002" cross-sections), decrease in power consumption and increase in performance seen in consumer and industrial products (Nomura, et.al., 1996), (Sarjeant, 1989). The ease with which they are integrated into designs and attached to printed circuit assemblies makes them a very attractive component to use for current and future circuit designs. They are inexpensive, have high capacitance, and are reliable (Nomura, et.al., 1996).

Even though these devices remain widely used, several manufacturing defects exist that limit the applicability of the capacitors. Defects occur both during and after the manufacturing process, however, detection of structural defects is extremely difficult, and very few solutions have been found for identifying defective capacitors. An overview of

the both the MLCC manufacturing process and a history of defect detection in these devices are presented.

2.3.1 MLCC Manufacture and Internal Structure

The main internal structure of MLCCs is not complex (Sarjeant, 1989), (Prymak and Bergenthal, 1995). The structure consists of alternating layers of non-conductive ceramic and metal conductors, as shown in Figure 2-2. Adjacent conducting layers are connected electrically to opposite ends of the device, and the electrical potential is maintained between metal layers within the dielectric ceramic, usually a barium titanate ($BaTiO_3$) layer (Davis, et.al., 2000).

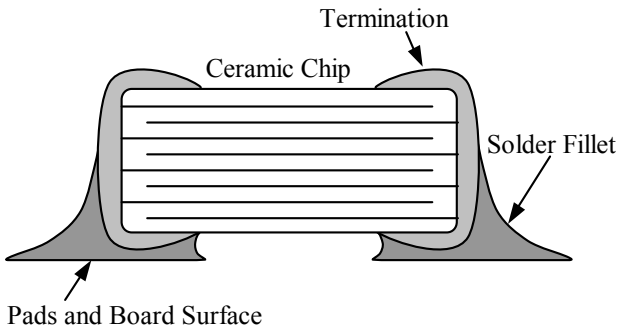


Figure 2-2: Multi-Layer Ceramic Capacitor (MLCC) Structure

The manufacturing process, shown in Figure 2-3 and simplified for brevity, consists of alternating processes (Nomura, et.al., 1996). A relatively large area is covered with a layer of ceramic slurry, and then a layer of metal paste is screen-printed over the green ceramic sheet to make the conductors for a batch of capacitors (Kahn and

Checkaneck, 1983). Another layer of ceramic is laid down, and the process continues until the desired number of layers and thickness has been achieved. At this point, the capacitors are pressed to remove voids, and then they are diced to create the individual devices. The green blanks are fired to cure the ceramic and melt the metal paste into a solid conductor. After firing, the end termination is created to connect the foil at each end of the capacitor to the appropriate terminal and to allow for easy attachment to a circuit board. The end termination is created through a dipping process into a metal paste. MLCCs from a single sheet of material are considered to be from the same batch, and screening tests are performed on each batch to ensure the proper internal structure and properties (Nomura, et.al., 1996).

2.3.2 MLCC Failure Mechanisms

Manufacturing failures do occur in MLCC devices. Voids and delamination can occur between the layers, caused by defects in the consolidation process. Chips, voids and thin layers can be caused during the dipping and firing processes. These types of defects are commonly caught through screening methods and accelerated life testing. Other types of defects are caused after properly constructed capacitors are attached to circuit board assemblies (Stevenson and Ewell, 1999). Many of these manifest themselves as cracks in the capacitor, and they are difficult to detect.

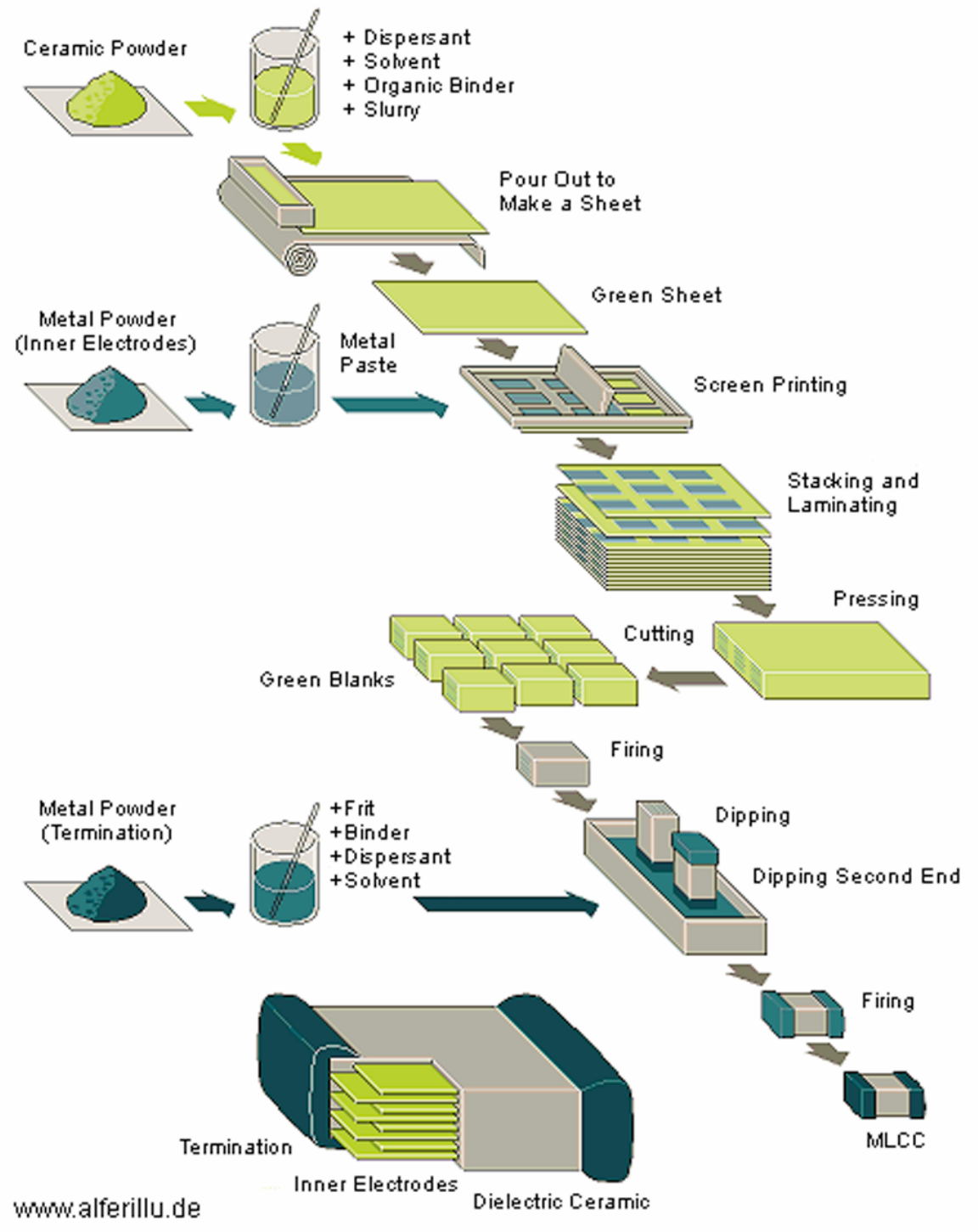


Figure 2-3: Manufacturing Process for Multi-Layer Ceramic Capacitors (MLCCs)

2.3.3 MLCC Cracking Failure Modes

Although several failure mechanisms exist for MLCC devices, the most common mechanism that occurs after placement is cracking, which is also the hardest mechanism to detect (Nomura, et.al., 1996). The root cause for cracking behavior can be traced to thermal and mechanical stresses that occur during the surface mount assembly process and environmental screening (Frieman and Pohanka, 1989), (Rawal, Ladew and Garcia, 1987). Because cracks occur when these environmental conditions are met, they cause reliability problems in the application of MLCCs (Cozzolino and Ewell, 1980).

2.3.4 Thermal Shock Cracks

Thermal shock causes scattered cracks in the thin layer of ceramic covering the body of the capacitor. These cracks can allow moisture and conductive particles access to the internal conducting layers of the capacitor, causing reliability problems with repeated power cycles. Thermal shock cracks accounted for 20-25% of total cracking failures when studied by Maxwell, (1988) and they were created because of a mismatch between the CTE of the capacitor and the circuit board. Often the "shock" occurs during the solder processing or cleaning processes, with wave soldering the most dangerous form of attachment because of the rapid change in temperature (Maxwell, 1988) (Rawal, Childs, et. al., 1988). Optimization of the material properties and capacitor geometry helps reduce the thermal shock problem, however, it does not completely prevent cracks (Rawal, Childs, et.al., 1988). Koripella (1991) studied thermal stress gradients causing the onset of thermal cracks, in an attempt to define parameters to eliminate this cracking mode. Specific temperature gradients were found, so to eliminate the gradient a pre-

heating stage was implemented to slowly bring the capacitor to a higher temperature before reaching the full reflow temperature. With appropriate pre-heating, the thermal gradient can be minimized, however, wave soldering still poses a threat to capacitor attachment (Faucett and Hogan, 1994). For large packages, the problem is more prevalent, and other factors, such as accurate temperature measurement during preheating and capacitor color, make preheating a difficult process to control.

Although advances in ceramic and capacitor packaging have helped minimize the problem, the low thermal conductance of MLCC packages makes thermal cracks a persistent problem. The thermal shock failure of MLCC components was investigated for MLCCs of different sizes ("0402," "0603," "0805," and "1206"), and smaller devices were more resistant to thermal shock than the larger ones (Chan and Yeung, 1993). The smaller size represents less thermal mass to overcome during preheating and soldering processes. Therefore, dangerous thermal gradients are not established under normal circumstances. Because of the reduction in size and power requirements for electronics packages, smaller devices have become the most popular, further reducing the occurrence of thermally induced cracks.

2.3.5 MLCC Flex Cracking Failures

Post-attachment manufacturing processes also cause cracks to form in newly soldered devices (Maxwell, 1988). Flex cracking stems from excessive mechanical bending of the circuit board during manufacture. Processes that can cause cracking include, but are not limited to the following: pick and place machines, board depanelization, board warpage during reflow, test fixtures, installation of connectors, and

final assembly (Maxwell, 1988). These processes cause flexure and vibration in the assembled circuit board, and when the mechanical stresses exceed the strength of the ceramic, a crack is initiated under the end termination and propagates at roughly 45 degrees from vertical, as shown in Figure 2-4 (Prymak and Bergenthal, 1995). These cracks can break through more than one layer of conductive material, causing a loss of overall capacitance. Because these cracks occur only under the MLCC package, near the end termination, detection of these cracks is very difficult. Therefore, in spite of the prevalence of these cracks in consumer products, not many detection methods can identify the presence of these cracks. Electrical tests in the factory may even indicate correct performance, but the cracks will eventually cause reliability problems in the field.

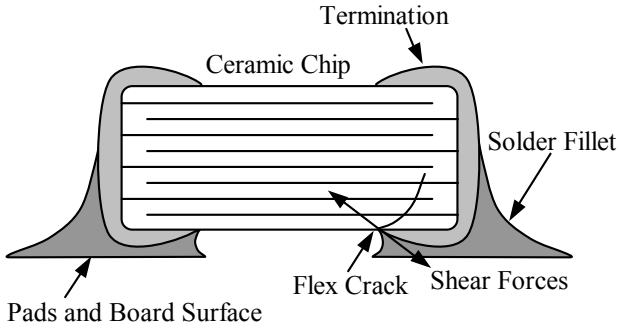


Figure 2-4: : Flex Crack in an MLCC Package

2.3.6 Screening Testing

Because there are so many failure mechanisms, screening mechanisms have been implemented for electrical and thermal/mechanical failure mechanisms, and the methods are applied to lots of parts right before attachment. Electrical screening ensures that

insulation resistance (performance) failures are screened out, by sampling a lot and testing the MLCCs at higher than normal operating conditions. Munikoti and Dhar, (1987) also proposed a highly-accelerated life test (HALT), which provides mechanical screening in addition to the electrical screening. By biasing the capacitors at eight times the operating voltage in a high-temperature chamber, proof testing of an entire lot is achieved in 48 hours, instead of the previously standard 1000-hour test. Because of the nature of both high-voltage and low-voltage failures, the HALT test also prevents the low-voltage failures because the screening method accelerates the defects that cause both types of failures (Munikoti and Dhar, 1988), (Mogilevsky and Shirn, 1988). Ingalls (1988) combined electrical and thermal testing procedures to show that the failure mechanisms were independent, but only under certain conditions. In addition, the accelerated testing parameters were checked, and they were not necessarily correct in the limited testing available. Although the use of screening tests does identify batches of capacitors with defects, simply screening by measuring a subset of the total batch inevitably leads to missed defects.

2.4 MLCC Previous Inspection Methods

Previous attempts to nondestructively detect defects in MLCC devices have shown the need for a more reliable technique. Several other techniques have been applied, and although they have each shown success with specific types of defects, no single solution has been found. The following discussion provides an overview of the previously attempted non-destructive testing performed on MLCCs.

2.4.1 MLCC Radiography

Radiography is the study of the loss of transmission of high-energy beams through materials, causing changes to the exposure of a film. Changes in the density of a material produce changes in the absorption rate of the energy, but the absorption rate in air is very small, making the detection of cracks and delaminations difficult. X-ray radiography has been used to successfully detect defects in MLCCs (Spriggs and Cronshagen, 1976). However, resolution was limited to large defects, 30% of the parts' overall geometry and 25 μm thick. Neutron radiography was also used to successfully detect delamination defects down to 0.5 mm in length and 5 μm thick after application of special fixtures, selection of a specific radiographic film, and use of electronic edge enhancement techniques (Cozzolino, Galvagni and Ewell, 1978). In addition to all the improvements to standard radiography techniques, the MLCC packages were left unterminated, so the metal termination did not obscure the radiography. Radiography does not seem to be applicable to online defect identification for MLCC packages, as shown in the literature.

2.4.2 MLCC Acoustic Microscopy

Acoustic microscopy is the application of transmitted ultrasonic energy to defect detection. Love and Ewell (1978) used a scanning laser vibrometer system to measure ultrasonic transmission at 100 MHz through a water tank and the bottom of a capacitor, immersed in the tank, to the top surface of a mirrored glass plate. Delaminations and erratic electrode stacking were detected with this method, and it was determined to be more sensitive than the X-radiography or neutron radiography (Love and Ewell, 1978).

A modern Scanning Acoustic Microscope (SAM) was used to find a large delamination in an MLCC package (Bechou, Ousten, and Danto, 2001). This system uses a focused 50 MHz ultrasonic immersion transducer and the pulse-echo method of inspection to record reflected sound from surfaces within the specimen. Time-frequency analysis of the complex time-of-flight information was necessary to accurately determine the depth of the defect because the multiple echoes caused by a multilayer structure complicate signal analysis (Bechou, Ousten and Danto, 2001). As far as online detection is concerned, neither of these methods is sufficient because the MLCC must be immersed in water for proper coupling. In addition, only horizontal delamination defects were located, and many of the cracks propagate vertically.

2.4.3 MLCC Acoustic Emission

When a crack occurs, the rapid release of strain creates acoustic energy, and the study of the detection and analysis of this acoustic energy is called acoustic emission (AE). A mechanical proof load was applied to capacitors in compression, and the acoustic emission was recorded with piezoelectric transducers (Kahn and Checkaneck, 1983). After being subjected to the AE compression test, the devices were subjected to a thermally accelerated life test, and the devices with more AE events failed much earlier than the other devices (Kahn and Checkaneck, 1983). The researchers admit that the AE test may adversely affect capacitor life.

To avoid the mechanical loading condition, Chan and Rawal (1988) used a voltage load in conjunction with AE testing to determine reliability. Both destructive physical analysis and thermally accelerated life tests were used to determine the

reliability of this technique, and the final determination of the study was that voltage-stimulated AE works well for detecting delaminations (Chan and Rawal, 1988). Both methods of AE did detect some defects in MLCC packages, but no work was performed on specimens with pre-existing flex cracks. Furthermore, both techniques require a severe loading condition, either voltage or mechanical, to generate the AE events, potentially reducing the lifetime of the capacitor.

2.4.4 MLCC Electronic Speckle Pattern Interferometry

Because of the restrictions on other methods, a noncontact method is desired for defect detection in MLCC packages. Electronic speckle pattern interferometry provides a noncontact method where laser illumination is used to create a speckle pattern on the specimen surface. Changes to the surface of the specimen cause the speckle pattern to change, and a comparison of two images from one device, before and after loading, leads to detection of defects that cause changes in deformation or displacement (Chan, et.al., 1993), (Chan, et. al., 2000). This method uses an electronic loading to provide a slight change in the image necessary for defect detection (Chan, et.al, 1995). Use of this method allowed the imaging of thermal shock cracks, but required the application of the electrical load for several minutes (Chan, et.al. 1995). Improvements to the system were made to improve correlation algorithms and decrease throughput, and detection of surface distortions down to 20 nm were possible (Chan, et.al., 1998). The implementation of wavelet packet noise reduction techniques further refined the resolution of the system, but the throughput for maximum resolution was still a hold time of 10 min under the electronic loading condition (Chan, et.al., 2000). Because this

method requires an electronic loading and hold time, implementation on a consumer electronic package would be difficult.

2.5 Vibration Modal Analysis Approach

Even though other inspection systems have been inadequate, an approach, based on vibration modal analysis, has potential to succeed. Previous inspection systems operated on the principle of sending energy (x-rays, ultrasound, etc.) into a system and watching for changes in the energy as it interacts with defects. Defect resolution is then related to the size of the waves propagating through the system with respect to the size of the defects or to the spatial resolution of the device used to measure the changes. However, the system being developed takes a different approach, relying on the dynamic response of a system to an impulse of energy to diagnose the presence of a defect.

Characteristics of the dynamic response are found from analysis of the equation of motion of a system, and a multi-degree-of-freedom system has the general equation of motion, shown in Equation 1-1 (Ginsberg, 2001):

$$[M]\{\ddot{q}\}+[C]\{\dot{q}\}+[K]\{q\}=\{Q\}-\{F_0\} \tag{2-1}$$

The elements of Equation 2-1 are [M] the mass matrix, [C] the damping matrix, [K] the stiffness matrix, and {q} are generalized coordinate vectors for displacement, velocity and acceleration. The right hand side is composed of force terms, where {Q} is the generalized force vector and $\{F_0\}$ is the vector of forces at static equilibrium. If [M], [K], and [C] are diagonal, then coupling of the generalized coordinates is avoided.

For an undamped system with no forced response, [C]=[0] and {Q}={0}, so the equation of motion reduces to Equation 2-2

$$[M]\{\ddot{q}\}+[K]\{q\}=0 \tag{2-2}$$

which leads to a solution in terms of a trial form with the assumption that behavior will be similar to a harmonic excitation. The trial form is shown in Equation 2-3 as follows:

$$\{q\}=\mathrm{Re}\left[B\{\phi\}\exp(i\omega t)\right] \tag{2-3}$$

where B and {ϕ} are constants (Ginsberg, 2001). The system can now be reduced to Equation 2-4 because to satisfy the original equation, only the coefficients change. Therefore, terms, such as B and the exp(iωt), are removed, leaving the general eigenvalue problem.

$$\left[[K]-\omega_j^2[M]\right]\{\phi_j\}=0 \tag{2-4}$$

In this formulation, ω_j is the j^{th} eigenvalue, or natural frequency of the system, and $\{\phi_j\}$ is the j^{th} mode of free vibration, or eigenvector, of the system (Ginsberg, 2001). The two quantities together describe a condition where harmonic excitation at a natural frequency will create a resonant response. The mode vector at that specific resonant mode describes the displacement of the surface of a vibrating structure.

Measuring and quantifying changes in the dynamic response of a system subjected to an impulse force (or other forces) can be performed through modal analysis, and it is the fundamental principle guiding development of the inspection system. Once a system is subjected to a broadband excitation from an impulse, it will vibrate until rest with resonance at the natural frequencies. Changes in the structural properties, such as stiffness, damping ratio or mass will change the impulse vibration response of a system. Taking a modal approach to structural defect detection removes the dependence on imaging a specific defect.

The structural properties for a device-solder-substrate system can be affected by common manufacturing defects. For the purposes of this research, the solder bumped devices are viewed as a mass or plate, connected to a rigid substrate with flexible solder connections that are the major source of changes in stiffness and damping ratio. A missing or disconnected solder bump will change the stiffness of the system, and a cracked or damaged device will change the mass and/or the stiffness of the system. If the input force, caused by the pulsed laser ultrasound generation, is consistent, then two good devices should behave similarly, if they are both made the same way (Liu, Erdahl and Ume, 2000).

Previous development work with this system led to the application of the error ratio algorithm by Sheng Liu (2000). This is a simple error summation method of comparing two vibration responses in the time domain, and it is presented in Equation 2-5.

$$\text{Error ratio} = \frac{\int [f(t) - r(t)]^2 \, dt}{\int [r(t)]^2 \, dt}, \tag{2-5}$$

In this equation, f(t) is the measured response, and r(t) is the response of a reference device. The value computed is zero if the waveforms are a perfect match and a positive value for any other comparison. This algorithm is used as a basis for much of the experimental work, as it provides a fast measure of the similarity of two signals. A fast algorithm for comparison is necessary to end up with a system that is capable of online inspection. A pattern recognition method was also applied to previous samples, allowing identification of good and defective chips as well as classification of two types of defects (Liu, 2002).

2.6 Laser Ultrasound

In order to create the bulk vibration of the chip necessary to compare vibration signatures, a non-contact method must be used. The method must be easy to control and implement, as well as be completely nondestructive. To fulfill the requirements, a technique called laser-generated ultrasound was chosen. This technique is safe, easily controlled through brief laser pulses, and very repeatable. The duration of the excitation is brief, so the source generates a broadband impulse excitation, allowing for excitation of a large number of natural vibration frequencies.

When a metal surface is irradiated with pulsed laser energy, an ultrasonic signal can be generated (Scruby, C.B. *et al*, 1990). The laser heats the surface of the sample, causing local expansion and contraction, which in turn generate stress waves in the

sample. For low absorbed fluxes, the surface where the absorption occurs never exceeds its melting temperature and the source of ultrasound is then a transient dilatation. The stress associated with this dilatation is for the most part below the elastic limit, and this mode of generation is referred to as thermoelastic. This thermoelastic source radiates both shear and longitudinal waves, as seen in Figure 2-5. At very high fluxes, the surface temperature rise is capable of exceeding the vaporization temperature (Sanderson, T., Ume, C., and Jarzynski, J., Oct., 1998). In this case, atoms leave the surface at high velocities imparting a momentum to the sample surface, and it is the momentum of particles leaving the surface that causes the ultrasonic signal to be generated. This mode of generation is referred to as ablation, and enhances longitudinal wave generation (Sanderson, T., Ume, C., and Jarzynski, J., Mar. 1998) (Hopko, S., and Ume, C., 1999).

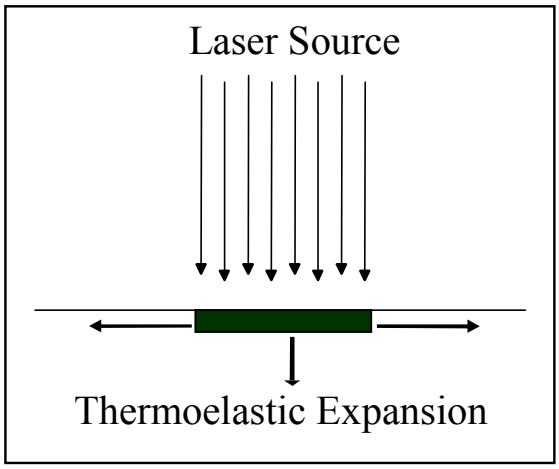


Figure 2-5: Thermoelastic Generation of Ultrasound

The thermoelastic mode of wave generation will be used in this research instead of ablation, because ablation does cause some damage to the surface. This can be accomplished by the use of either a single laser beam or a laser array (Jarzynski, J. and Berthelot, Y. H., 1989). A Q-switched Nd:YAG laser with a wavelength of 1064 nm is used as the laser source, as it is a common method of creating laser ultrasound (Hopko, S., and Ume, C., 1999). When the laser pulse is incident on a surface, part of the incident energy is reflected and the rest is absorbed. The expansion and contraction of the surface caused by the laser pulses is the source of a stress wave, creating ultrasound.

For larger chips, more energy may be required to stimulate vibration modes for the entire chip. In this case, a fiber array may be used to avoid ablation (Yang, J. and Ume, C., 1994). Using an array of fibers spreads the energy out to a larger area on the specimen, thus preventing ablation and subsequent damage of the delicate chips. An alternative a fiber array is to use a focusing objective to control the energy density over a larger single circular area, keeping the density below the threshold that causes ablation (Howard, Erdahl and Ume, 2002). In addition, the laser source can be moved to different locations on the surface of the device, making the excitation method even more effective for generating vibration modes.

2.7 Finite Element Analysis

For the complex geometry in the attachment of an SMT component to a circuit board, analytical solutions for the vibration response are difficult to develop. Although attempts have been made to use the superposition method or the Ritz method to find analytical solutions for a vibrating plate (similar to an IC chip), the complex boundary

conditions created by the high number of connections are a major roadblock in finding a closed-form solution (Gorman, 1982). Therefore, the most effective way to create a model of the vibration behavior is to use a finite element model (FEM) approach for vibration modal analysis. By breaking the system into small, discrete components an approximate solution can be found that provides valuable insight into the behavior of physical components, allowing inspection of the natural resonant modes, the associated eigenvectors and the changes that occur in these values as simulated manufacturing defects are introduced to the model through changes in geometry or boundary conditions.

The basic steps to create a finite element model are as follows:

1.) Create a 3D model to represent the structure in question, taking advantage of any symmetry that is applicable. For the case of the devices in question, symmetry would apply up until the point that a simulated defect is added. Then, there are no planes of symmetry to allow simplification of the problem. A full 3-D model must be implemented to directly compare perfect and defective conditions simply by changing the boundary conditions.

2.) Create a mesh of the model using appropriately selected elements. A large variety of elements exist for specific purposes, structures and loading conditions. Elements must be selected based on knowledge of their limitations and their ability to emulate the physical aspects of the system. The elements are assigned all the relevant material properties: Young's Modulus, density, and Poisson's ratio. These values are published in literature, they may be provided by the manufacturer, or they can be experimentally determined.

3.) Apply appropriate boundary conditions. This includes loads, constraints and restrictions on behavior. For a modal model, loads are ignored, as the calculation of natural frequencies assumes a free vibration response. For the assumptions that have been stated about the behavior of the system, the bottom surface of the solder bumps will be considered to be fixed in three dimensions.

4.) Assemble a global stiffness matrix, and solve for the nodal values of each element. Output includes the natural frequency of each vibration mode and the associated eigenvectors.

5.) Post-processing is the step where the data is analyzed and put into meaningful terms for comparison with experimental values, allowing verification of the model's behavior.

Results obtained from this method are only approximate. However, FEM models allow for rapid changes, creating an opportunity to test different loading conditions, material properties or geometries. Trends in behavior can help identify trends to search for in experimental data.

2.8 System Identification

In order to provide a link between experimental and modeling results, some of the data must be extracted to allow proper comparison. Since the FEM analysis produces modal properties, an evaluation of the modal properties extracted from experimental data will validate the fundamental behavior of the system.

Van Overschee (1996) developed one simple method of identifying system parameters. Based on a State Space System Identification Algorithm, the algorithm implements a system model for a stochastic system that does not require explicit knowledge of the system input. The model of the discrete system using finite difference notation is:

$$\begin{aligned} x\_\{k+\} &= Ax\_k + Ke\_k \\ y\_k &= Cx\_k + e\_k \end{aligned} \tag{2-6}$$

where the matrices (A, K and C) and the data (x_k and e_k) are referring to discrete, sampled data. The discrete values can be converted back into a continuous system, as shown in Equation 2-7, which converts the matrix and solves for the eigenvalues in MATLAB.

$$\lambda = \frac{\ln\left(eig\left(A\right)\right)}{\Delta t} \tag{2-7}$$

Although the algorithm is slow and may be inaccurate for closely spaced vibration modes, it does aid in automating the data analysis. From the complex eigenvalues extracted from experimental data, through finding the eigensolution to the [A] matrix, the natural frequencies and damping ratios are readily calculated. The complex eigenvalues are defined as:

$$\lambda = -\zeta\omega_{nat} \pm i\omega_d \tag{2-8}$$

Then, the natural frequencies are computed from the magnitude of the complex eigenvalue as:

$$\omega_{nat} = \sqrt{(\zeta\omega_{nat})^2 + (\omega_d)^2} \tag{2-9}$$

Similarly, the damping ratio is determined from the complex eigenvalues. The equation is as follows:

$$\zeta = \frac{-(-\zeta\omega_{nat})}{\|\lambda\|} \tag{2-5}$$

This calculation is simply the real part of lambda divided by the magnitude of the complex eigenvalue (lambda). The calculations are somewhat simple, but the information is essential to the successful comparison of the FEM model with the experimental data.

A fundamental comparison between the natural frequencies from the data and in the FEM model can show that the structure will have the same vibration response. If the frequencies are the same, then the systems will have the same response. In order to get an accurate transient response model, the modal damping ratios extracted from the data can be applied to the matching modes from the model. For modes that were not experimentally identified, the modal damping ratio can either be assumed to be close to one of the identified modes, or the ratio can be set to a high value to minimize the effect of that mode on the final response.

2.8 Modal Assurance Criterion

To compare the modal characteristics from experimentation and modeling, the modal assurance criterion (MAC) is used (Allemang, R. 2002). This method compares the eigenvalues and eigenvectors estimated from an experimental frequency response function to analytical results. Other methods for comparing the mode shapes exist, such as an orthogonality check, and these methods provide an alternative to the MAC value. However, all of these methods rely on a mathematical combination of the modal vectors to provide a measure of how well they match each other.

An orthogonality check is one of the most basic methods of comparing the mass matrix and mode vectors from a finite element model to experimental values to check for validity. If it works correctly, this method validates an experimental estimation of modal vectors with a model, but it can couple the errors in both the analytical and experimental modal vectors into one approach, making it difficult to tell where the problem is when it fails (Allemang, R. 2002).

Therefore, the modal assurance criterion (MAC) is the method of choice for comparing the modal parameters from two sources. The MAC calculation produces a statistical indicator of the correlation between two modal vectors (Allemang, R., 2002). The criterion relates the degree of consistency between two modal vectors as a scalar constant, using one as a reference, and it is shown in Equation 2-6 (Allemang, R., 2002).

$$MAC_{cdr} = \frac{\left|\{\psi_{cr}\}^T \{\psi_{dr}^*\}\right|^2}{\{\psi_{cr}\}^T \{\psi_{cr}^*\}\{\psi_{dr}\}^T \{\psi_{dr}^*\}} \tag{2-6}$$

In this equation, $\{\psi_{cr}\}$is modal vector c at mode r and $\{\psi_{dr}\}$ is modal vector d at mode r, and modal vector d is used as the reference. The equation produces a scalar value between zero and one. A value of zero indicates no correspondence, while a value of one indicates perfect correspondence. Application of this criterion is a convenient way to measure consistency, so it will be a valuable tool for comparing experimental results to each other and to the FEM model results.

2.9 Justification

Although broad spectrums of destructive and nondestructive techniques have been used for both flip chip and MLCC packages, a new approach is needed to fill the void in the capability of current systems. The laser generated ultrasound excitation technique, coupled with non-contact measurement of vibration provides a new alternative to the traditional methods of searching for defects. Using a modal analysis approach, the vibration modes of the package-substrate system are extracted and compared to the same modal properties found from a finite element analysis. The individual components of this process have been used before, but a structural analysis approach is a new method for detecting manufacturing defects in electronic components.

CHAPTER III

INSTRUMENTATION AND EQUIPMENT SETUP

In order to generate the data needed for analysis, a laser ultrasonic inspection system was used. This system is comprised of a laser source, a laser pulse delivery fiber with optics, a heterodyne interferometer, a positioning system, an alignment system and a data acquisition system. Interface with the system is made through software that was written specifically for this project. All component interaction with the test specimens, flip chips and MLCCs, are non-contact and nondestructive. This system is the result of development efforts by Erdahl (2000), Liu (2001) and Howard (2003).

3. 1 Instrumentation

The inspection system was designed to allow flexibility in configuration and to keep the necessary components simple, reliable, and robust. Only three main subsystems are required for the test setup: a source of ultrasound, a fixture to hold and move the sample, and a sensitive instrument to record the sample's vibration. Other components aid in these processes, such as a digital camera, a fiber optic coupling cable, motor controllers and a vacuum fixturing system. All of these components are tied into one computer, which manages data acquisition and processing, controls the pulses from the

laser, controls the sample position, and interfaces with the secondary subsystems. Figure 3-1 contains the layout and setup for this inspection system.

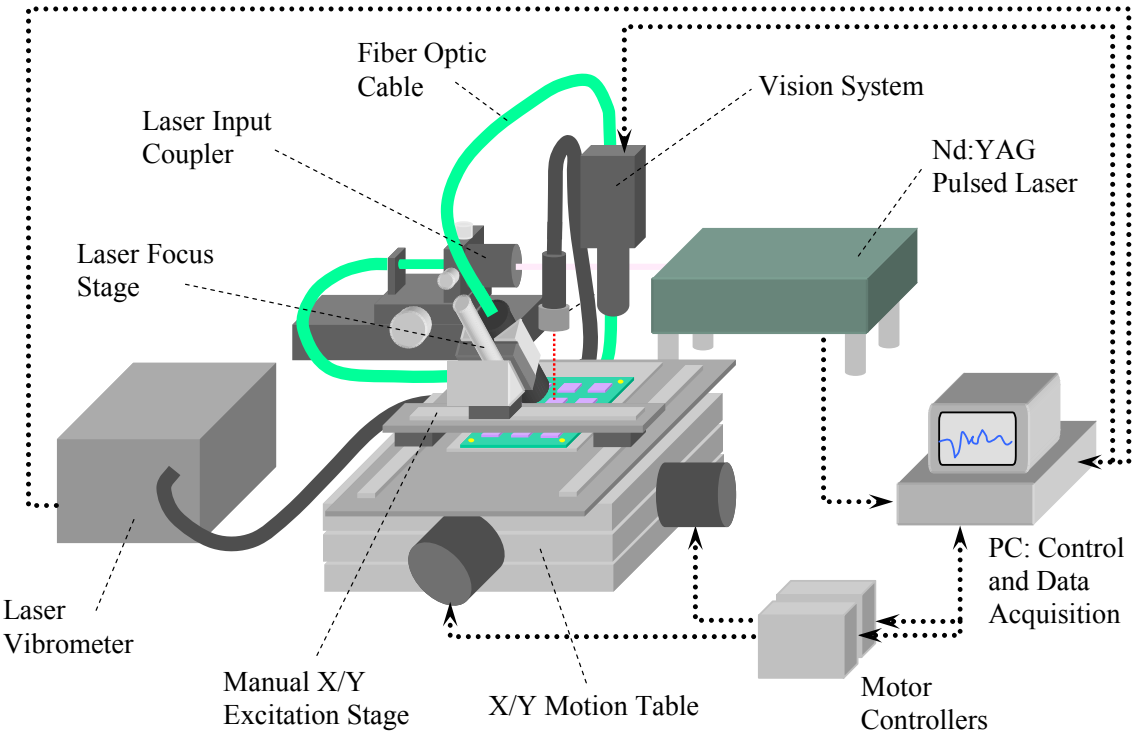


Figure 3-1: Laser Ultrasonic Solder Joint Quality System

3.2 Ultrasonic Source

The specimen is excited into vibration using laser-generated ultrasound. Ultrasound is generated in the specimen by pulses of an Nd:YAG infrared laser from New Wave Laser. The laser has a maximum power output of about 45 mJ/pulse, or 900 mW, at a wavelength of 1064 nm for a 3.2 mm diameter beam. The pulses are fired at a

user-selectable rate of up to 20 Hz, which allows adequate time for recording the vibration signals and for the specimens to return to the rest state between pulses.

The laser launches energy through a fused-silica optical fiber to the test sample, using focusing optics to couple the laser pulses into the fiber and to collimate the laser pulses at the distal end of the fiber (Howard, 2002). The optical fiber has a core diameter of 400 μm, and the focusing optics allow the collimated beam to be in the range of 0.6-8.0 mm^2 with a standoff distance of greater than 50 mm (Howard 2002). Using the fiber helps limit the power transmitted, allows extreme localization of the energy, allows the test fixture to be moved without losing alignment, and the focusing optics are useful for controlling the energy density of the excitation spot on the surface of the specimens.

Although the maximum rated power for the laser is 45 mJ/pulse, the power transmitted through the fiber is kept to about 2.5 mJ/pulse through the use of an optical attenuator inside the laser. This incident energy is enough to cause the specimens under investigation to vibrate, but it is low enough to prevent damage to the optical fiber. Larger chips will require more energy to excite bulk vibration modes, so in that case an array of fibers could be used to produce more ultrasound without exceeding the damage limit of the fibers or the specimen.

To keep the fiber out of the field-of-view of the fiber interferometer, the laser pulses are incident on the surface of the specimens at an angle of 45º, as shown in Figure 3-2. The angle also keeps any reflected infrared energy from entering the sensor for the interferometer and potentially causing damage. A manually adjustable x-y stage allows the fiber to be aligned correctly at 45º with a specific point on a specimen's surface,

usually the center of the device. The focus at the distal end is adjusted using a manual stage to adjust the position of the lens on the 45º stand. The interferometer head is positioned directly over the chip and aligned normal to the surface in order to get the best possible signal from a specimen's surface.

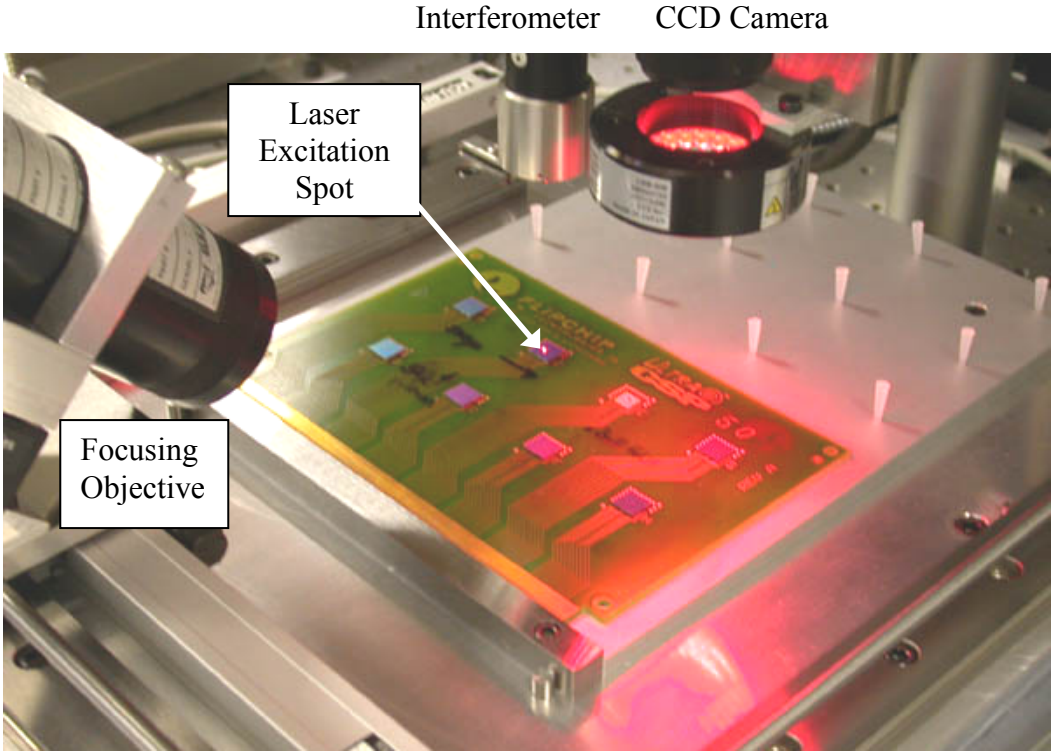


Figure 3-2: Fixturing for Board Inspection

3.3 Precision Positioning

The fixture for holding the specimen allows the interferometer to take measurements at different points on the chip's surface. An alignment fence is used to roughly position each sample, and the circuit boards are aligned using a CCD camera to find the location and orientation of features on the specimens. The CCD camera allows

identification of the specimen location within about 1 μm. The fixture, with numerous vacuum holes to hold the samples in place, is mounted on top of an XY-positioning table with a repeatability capability of ±10 μm over 100 mm of travel. The stages have a pre-loaded lead screw to minimize backlash, and the stages have a 5 mm pitch on the lead screw threads. Standard NEMA 23 stepper motor mounts on the ends provide a connection point for DC stepper motors controlled from the computer.

Stepper motors and smart motor controllers are used to drive the stages. The motor controllers are the DM-224i Intelligent Microstep Controller/Drivers from API Controls, Incorporated, as shown in Figure 3-3. All of the inputs and outputs are optically isolated for protection, and the drives accept a 12-48 VDC input range. Using the power provided from a DC voltage source, the drives can deliver a 3 A maximum output. Each controller is individually addressable through the RS-232 serial communications port on a computer and has the ability to store control programs in flash memory. By taking advantage of these features, the automation program was simplified. Control commands for the desired position were sent to the controllers, saving the effort of controlling the stepper motors directly through software. The stepper motors are controlled in an open loop configuration, and positioning is achieved through counting pulses sent to the motors.

Stepper motors that matched the controllers were selected. The motors are model M231-03 from API Controls. These motors have the NEMA 23 connection to match the stages and are 3 VDC, 2 A microstepping motors. The motors plug directly into the controller and get both the stepping sequence and power from the controller. Using this

stage assembly, the position is accurate to about ±0.010 mm. Errors in position can be introduced through manufacturing variation of the specimens on the surface of one board to the next. Leaving these components adjustable adds flexibility into the system, allowing for performance optimization.

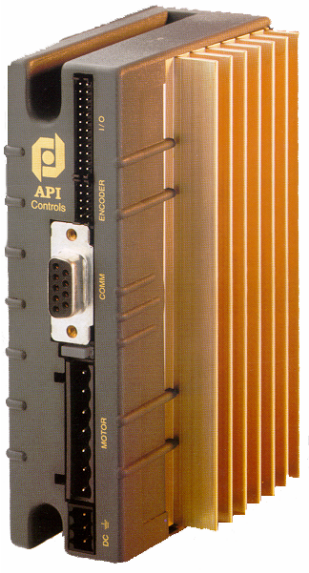


Figure 3-3: DM-224i Intelligent Microstepping Driver (API Controls, Inc.)

3.4 Vibration Measurement

To measure the surface displacement at specific points, a fiber head interferometer is held in a fixed position over the testing area. Alignment of the fiber head is very critical, but focusing optics on the head allow for a larger standoff distance that allows an unobstructed measurements at any point on the specimen surface. By moving the specimen instead of the interferometer, there is less opportunity for the interferometer to become misaligned from a perpendicular position relative to the surface

of the chip. Loss of a perpendicular incidence on the location of the interferometer to the specimen surface will cause the loss of a good vibration signal.

The interferometer was purchased from Polytec Incorporated and is a model OFV-511 heterodyne fiber interferometer with an OFV-2700 Ultrasonics Vibrometer Controller, as shown in Figure 3-4. The interferometer measures the displacement of the surface, and the vibrometer controller contains electronics to provide an analog signal for data acquisition. The controller has a high pass filter to reject low frequency noise below 25 kHz and a maximum bandwidth of 20 MHz, making the instrument useful for an extremely large bandwidth. The maximum range for displacement measurements is 75 nm while the minimum detectable displacement is approximately 0.10 nm. Therefore, any change in the solder joints that cause a change in the surface vibration of at least 0.10 nm will be detected by the system, giving the system a high resolution. However, this resolution is highly dependent on the noise level in the signal. As long as the noise is minimized through optimal alignment with the specimen, the measurement limit will be close to the actual limit during experimentation.

Figure 3-4: Polytec Interferometer

3.5 Data Acquisition

The signals from the interferometer are recorded using a high-speed data acquisition card purchased from GaGe Incorporated. The card is model number 8012A/PCI, and came as a two-board set. The A/D converter plugs into an ISA slot on the computer and the data transfer card plugs into a PCI slot. At the fastest acquisition rate, the card can take 100 million samples per second (MS/s) with a resolution of 12 bits on one channel. When two channels are used, then the maximum acquisition rate is 50 MS/s. The board comes with C++ drivers for Windows, allowing development of an automated program to control the entire system. The data capture, motor control and analysis can all take place in one program. By acquiring the data directly to the computer, the data can be analyzed immediately.

3.6 Automation Program

In order to control the system and tie all of the pieces together, a control program was needed. A program was written in Borland C^{++} Builder to control all aspects of data acquisition (Erdahl, 2000). The program controls all of the parameters on the data acquisition card as well as the positioning of the XY-stage. A screen capture of the program is shown in Figure 3-5. On the right of the image the trigger signal and a sample signal taken during acquisition are shown.

All of the controls are in the left portion of the window. In order to start acquiring data, the board must be initialized and configured. Using the controls at the upper left, the acquisition parameters can be set in a pop-up dialog box, shown in Figure 3-6. This dialog box allows the user to set single or dual channel, the sampling rate, the trigger settings, the scaling parameters, and the impedance coupling to use.

After initializing and configuring the board, the number of signals to average can be set and data acquisition can be controlled. In the bottom left corner of the figure, the controls for the XY-stage are seen. There are two sets of controls. One of them allows the user to manually control the path of the stage, and the other one allows the user to input a series of motions described as vectors. Using the automated series, data can be recorded at several points on the surface of the same chip in a very short time frame without any intervention from the user. The data files are recorded as ASCII text files that can be stored and read easily.

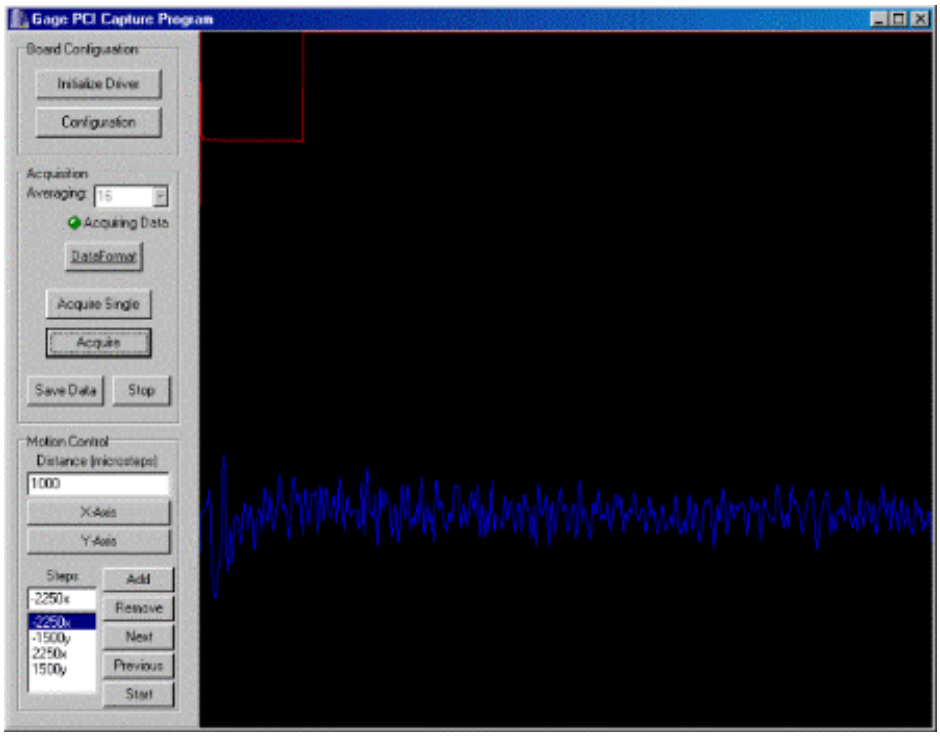


Figure 3-5: Screen Capture of Data Acquisition Program

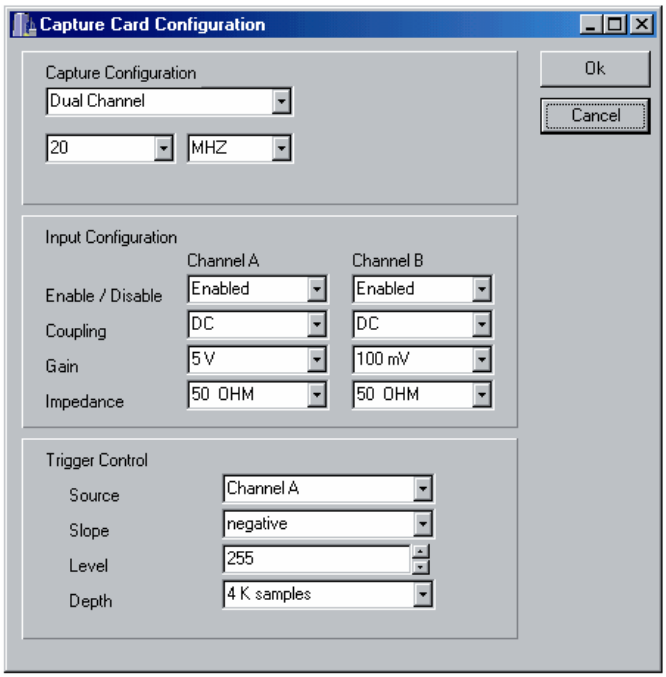


Figure 3-6: Screen Capture of Dialog Box for Setting Data Acquisition Parameters

All of the components used in the setup, from the ultrasonic source to the data acquisition program are adjustable, making the system flexible and allowing different types of tests necessary for adjusting the inspection locations to get the best results. The extremely flexible nature of the system allows the adjustment needed in the laboratory. Changes in the procedure, such as interferometer placement, excitation laser placement, and digitization parameters, must be set for each new specimen being tested. Details about the specific changes in procedures for each component are presented in the discussion for that component.

CHAPTER IV

EXPERIMENTAL PROCEDURES

For this research, the experimental procedures can be broken down into two distinct categories. First, the specimens must be selected, constructed and electronically verified. Then, the laser-generated vibration response data must be collected for analysis. Although the most important aspect of a procedure is consistency, the specimen creation was performed using two methods. The data collection was very consistent, however, minor variations in the procedure were necessary to accommodate validation procedures. The most general procedures are presented in this chapter, and small deviations from the procedures are presented in the chapters with the data the changes affect.

4.1 Specimen Creation Background

In previous work performed with the laser ultrasonic inspection system, many defects have been identified. Liu and Erdahl (2000) showed strong correlation between signals collected and defects such as missing solder bumps, cracked chips, misalignment and combinations of these defects with 14-bump flip chips mounted on ceramic substrates. Visteon provided the samples, and the defects were generated by hand. Howard (2001) presented data showing misalignment by one row in two orthogonal directions for a 98-bump CSP with a nearly fully populated array of solder bumps that

was mounted on an organic substrate. In addition, the laser inspection system was used to locate one missing bump in the corner of this same CSP package. Siemens carefully prepared the CSP samples for use with this inspection system, as a technician deliberately removed solder bumps from the chips prior to placement on the test boards.

In the manufacturing environment, however, missing solder bumps, damaged chips and misalignment are more commonly caught using less-sophisticated inspection methods. Solder bumps are automatically checked prior to placement by a pick and place machine, using machine vision to verify the presence of all bumps immediately before placing the device on the PCB. Machine vision can also be used to inspect for gross alignment errors and defects on the surface of the chips. The more common manufacturing defects are open solder joints. These defects occur because of a problem during reflow, and they may not be caught until after the underfilling process has taken place, since no convenient method has been found to identify these defects.

In order to determine the capability and the resolution of the current inspection system to identify open solder joints, another flip chip package has been chosen. The chip is a peripheral array, 6.3 mm square, 48-bump daisy-chain device. The bumps are 190 μm in diameter and are spaced with a pitch of 457 μm, with twelve centered on each side of the device, as shown in Figure 4-1. In comparison with previous devices tested with the laser vibrometry system, this device has a smaller pitch, smaller solder bumps and is readily available for use and assembly with current facilities.

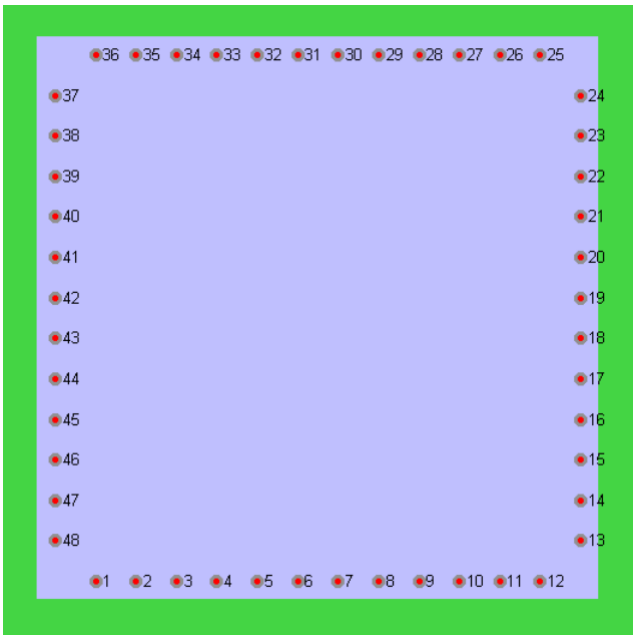


Figure 4-1: 48-bump Daisy-chain Peripheral Array Flip Chip Package (fb250)

4.2 Assembly Objectives

Before starting assembly, it is necessary to examine the process and the expected outcomes. The first goal in creation of these samples is to test the ability of the system to detect open solder bumps on samples with no underfill. To meet that goal, a variety of samples were created with open joints in different locations, such as near a corner or in the middle of a side. For a square peripheral array device, several symmetries exist that aid in simplifying the locations that need to be identified. Since the device is the same on each side, the extreme points that must be inspected are at the corners and in the middle of a side. Therefore, a test vehicle with chips having open bumps in the corners of an edge and open bumps in the middle of a single side was created to test the resolution of the system.

4.2.1 System Resolution

Before performing tests to measure the resolution of the system, the type of resolution that can be measured for this system must be defined. Traditional nondestructive evaluation methods (AXI, C-SAM) employ a full scan of the surface of the entire specimen, so the resolution of such systems is based on the spatial resolution in the X-Y scanning plane and the spatial resolution of the probe (Semmens, 2000), (Bechou, et.al., 2001), (Lehman, 2002). Defects larger than the spatial resolution can be detected, as the change in response over a single point indicates a change in the signal. Therefore, the major emphasis in development of those systems is focused on decreasing the minimum spatial resolution through a combination of more accurate positioning stages and better control of the x-ray and ultrasonic propagation (focal characteristics).

For the current system, only selected inspection points were used to determine the quality of attachment, replacing the idea of a full-field raster scan. Defect resolution is not as strongly tied to the spatial resolution of the scanning system, as it is in the traditional systems. Instead, the resolution is based on the capability of the system to measure a change in the vibration response to the laser ultrasonic excitation force. Although the repeatability and accuracy of the stage is important to ensuring the same points are measured on different packages for comparison, the main factor in system resolution is the amount a given defect changes the vibration response. Changes in the vibration response are a function of the defect severity as well as the defect location.

Therefore, the current inspection system provides the ability to find some defects that are missed by existing systems, but a traditional approach to measuring resolution is

not going to work. Resolution is defined in terms of the smallest defect that causes a significant change in the vibration response to be consistently identified. Testing performed to measure resolution will be applicable to only one specific package size, and may only be applicable to one type of defect, such as open solder bumps.

With resolution defined as the number, size and location of intentionally created defects, the rest of the test plan was developed. As observed in previous testing, open defects are harder to identify than missing defects. Therefore, samples with multiple open defects adjacent to each other were constructed to simulate manufacturing problems. Up to three joints with open bumps adjacent to each other were used to demonstrate the resolution and capability of the inspection system.

4.3 First Flip Chip Sample Configuration

A test vehicle was designed to meet the goal of measuring resolution of the inspection system. A series of specimens with one, two or three open joints was specified. Two sets of specimens with these sequences of open bumps in different locations. One series starts from the corner of a chip, and one starts in the middle of one side of the chip, as shown in Figure 4-2. Another defective specimen was added to the board for completeness, and it has two open joints adjacent to each other. In this case, the joints are on two perpendicular sides of the chip. Combining these defective devices with three reference devices brings the total number of chips to 10. These can all fit on one PCB, so experimental error can be minimized by reducing the setup required to test batches of ten chips. Two boards were constructed to test repeatability and to allow a backup in case of assembly problems.

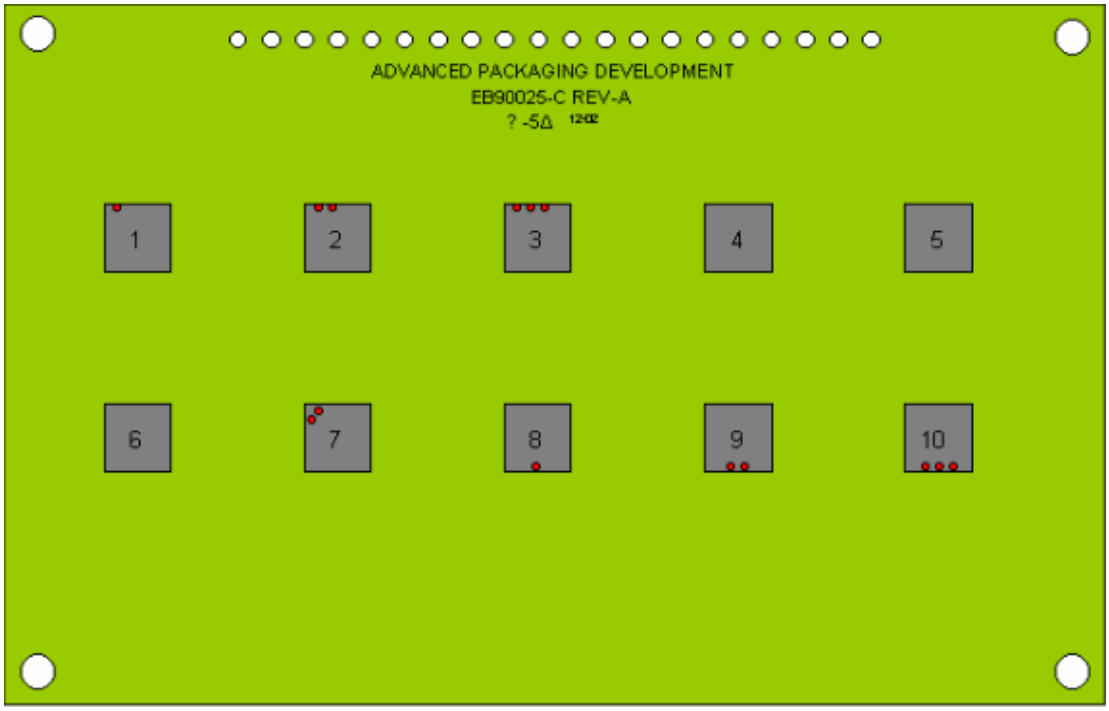


Figure 4-2: Plan for Construction of Flip Chip Specimens with Open Solder Joints

4.3.1 Manual Defect Creation

In order to create the opens in the most realistic way possible, solder mask was applied to selected solder pads on the surface of the bare PCB board. This method of creating defects simulates one of the ways an open can occur in a manufacturing environment, while still giving control over the placement of the defects. By protecting the solder pad completely from being wet by the liquefied solder bump during the reflow process, the certainty of creating the desired defect is very high.

4.3.2 Solder Mask

The solder mask used for this work was donated by members of the Packaging Research Center (PRC), and it is commonly used in the board fabrication process. The solder mask is produced by Taiyo America, Inc., and it is a two-part mask, having an ink and a hardener. The ink is Taiyo PSR-4000BV AUS5 Green Liquid Photoimageable Solder Mask for BGA Applications, and the hardener is Taiyo CA-40BB AUS2 Liquid Photoimageable Solder Mask Hardener. This combination "has been specifically designed for BGA, Flip-Chip and other Chip Scale Packaging (CSP) applications" (Taiyo, 2002). To get proper curing, the mixture is 100 parts of the mask to 43 parts of the hardener, and after application, a final cure process is necessary to ensure complete hardening and complete protection from solder adhesion for the pads. The recommended oven cure cycle from the Packaging Research Center (PRC) was 115 ºC for 60 minutes, but the Taiyo data sheet recommends 135 ºC for 45-60 minutes. However, conversation with the Taiyo technical support confirmed that the cure cycle recommended by the PRC would be adequate. The main difference is in the final hardness and material properties, however, the only concern in this situation is the coverage and prevention of electrical connection.

4.3.3 Solder Mask Application

Solder mask was applied to the bare pads on the test boards in small amounts to precisely cover the pads with a minimal amount of solder mask to ensure coverage. To prevent an electrical connection, the pads need to be fully covered, but in order to allow for minimum mechanical interaction between the solder bump and the PCB, the layer

needs to be as thin as possible. Although, the most ideal situation would be to create the solder mask defects during the manufacture of the board, the occurrence rate is too low to be useful for a controlled study. Simulation of the defects is more cost effective and easy to perform.

A Wentworth Laboratories microscope and mechanical stage setup was used to aid in hand-deposition of the solder mask on the appropriate pads. Small amounts of solder mask were transferred to the end of a thin metal probe that was attached to a three-axis microstage. Using a magnetic base, the probe was held in a fixed position while the PCB was moved under the microscope's viewing window. When the desired pad was in the viewing window through adjustment of the microstage, the probe with the solder mask was touched to the surface and moved along in at least three passes over the pad in order to cover the two sides and top of the pad, as shown in Figure 4-3.

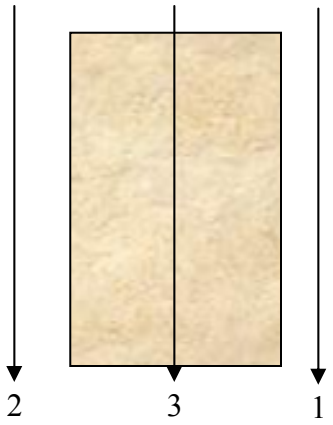


Figure 4-3: Scanning Pattern for Deposition of Solder Mask on Gold Pads.

The probe was touched to the surface of the board, and surface tension pulled the solder mask off the probe onto the board. The first and second pass were used to create a

fillet of material to seal and protect the sides of the solder pad. The final pass (or two) was used to cover the top surface of the pad, and to connect with the solder mask deposited on each side. Additional passes were used to touch up missed areas, and even out the layers of solder mask.

Although the process sounds simple in theory, the actual application was difficult. High viscosity and elasticity of the solder mask material made actual deposition in a smooth layer very challenging. The total time to cover the pads on one board was approximately six hours. The boards were then placed in an oven for the 1 hour cure time that was recommended.

4.3.4 Verification of Solder Mask Deposition

After the curing process, the boards were evaluated to ensure complete coverage had been achieved. As previously stated, the pads need to be completely isolated, and the solder mask layer must be thin to minimize the effect of the mask on the vibration of the chip. Therefore, two separate checks were made to evaluate the deposition coverage and thickness.

Digital pictures were taken at 8X and 25X magnification of all the pads that were covered. These pictures show the coverage of the individual pads, the fillets of solder mask, and the relative smoothness of each pad. Examples of these pictures are presented here in Figure 4-4 and Figure 4-5. Pictures in grayscale show some of the details, but the pseudocolor option available with the camera/microscope setup shows the outline of the solder mask fillets more clearly. The solder pad on the left in each picture is free of solder mask, representing the as-manufactured state of the board. The solder pads on the

right in the pictures show solder mask material completely covering the pad, and filling in the sides of the pad to prevent solder from attaching to the sides of the pad.

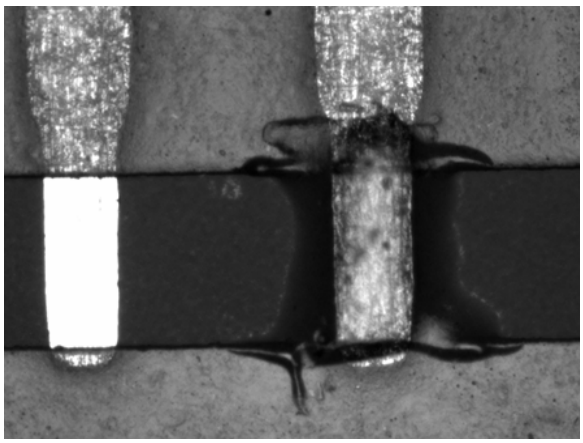


Figure 4-4: Representative Solder Pads Covered with Solder Mask.

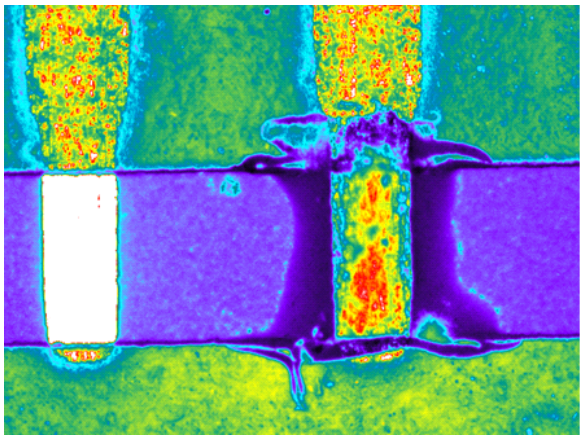


Figure 4-5: Representative Solder Pads Covered with Solder Mask in Pseudocolor.

After the shape and coverage of the pads was verified, a measurement was made of the change in height from the top of a standard (untouched) solder pad to the

maximum height of the solder mask covering the pads with simulated defects. For this purpose, profilometers provide a good measure of the relative change. A probe-tip profilometer was used to scan the surface of several pads to verify the deposition thickness.

Scans were taken across the solder pads, and the bare board is used as the reference plane. The scans show that the solder pads are between 20.84 μm and 22.19 μm thick, so the thickness is very consistent, as would be expected from a standard manufacturing process. The maximum height of the solder mask above the board was primarily in the range of 49.06 μm to 75.25 μm. However, one solder pad with mask applied had a height of 91.71 μm. Therefore, the solder mask thickness was between 29 and 55 μm thick.

4.3.4 Circuit Board Assembly

After special care preparing the PCBs for assembly, the assembly process is the same process typically used for these chips. These 48-bump chips are used as test chips for training new machine operators, so the assembly process is well-understood. First, the parts are placed on the circuit board, then the board is run through a reflow profile in an oven. Post-processing work was performed to ensure proper assembly had taken place.

Pre-bumped flip chips were loaded into a Siemens SIPLACE 80 F^5 pick and place machine, which was running a standard program to place the fb250 flip chips on the PCB used in this study. The program sequence has automatic routines to perform quality

checks on the components. First, it checks the fiducials on the board to ensure proper alignment, and then it checks each chip for the correct number of solder bumps using another camera before dipping the chip into flux and placing it on the board.

The flux used was selected for applicability to a wide variety of applications. Produced by Heraeus Circuit Materials Division, the V-369 flux was set to a 65 mil depth. Because the flux holds the flip chip in place, and because the pads for a flip chip are so small, there is no solder paste applied to the surface of the board prior to assembly. The solder bumps already attached to the chip are more than adequate to hold the device in place.

After the parts were placed on the board, the boards were run through a standard eutectic reflow profile. This profile hits a peak temperature of 230 ºC with appropriate heating and cooling rates to ensure proper connections are made. Following a return to room temperature, the individual connections for each of the solder bumps was tested for continuity, to assure that electrically open circuits were successfully created.

Although the assembled boards were successful in creating electrical opens, the bumps were not mechanically open. The deposition of solder mask over the pad deformed the bumps, and since the solder mask deposition was difficult to control, different amounts of solder mask were deposited on each pad, creating an inconsistency in the assembly process. These chips were used for initial testing of the modal excitation and data processing algorithms prior to the final set of samples. The results are presented in Chapter V. However, the chip construction process was not controlled well enough to

experimentally determine the measurement limit of the system and technique for open solder bumps.

4.4 Second Flip Chip Sample Configuration

To overcome the problems with the previous samples, a new batch of samples was created. The same test die (FB250, PB-18) was used, and the circuit board was very similar. However, the PCB design was modified to remove the solder connection pads from the desired positions to simulate open joints without the need to deposit solder mask with the desire to create a mechanically and electrically open set of samples. Two PCB designs were created. One of them, shown in Figure 4-6 shows the PCB design with a sequence of one to seven adjacent open bumps, starting at the corner of a chip. Figure 4-7 shows the same design, modified to have a sequence of defects from one to seven adjacent opens, centered on a side. The increase in the number of adjacent defects allows for characterization of the resolution of the system more clearly than before. Also, having separate boards for each defect allows characterization of the board-to-board changes for the reference chips. Three reference chips are intentionally left on each board to provide a strong baseline for comparison to the defective chips.

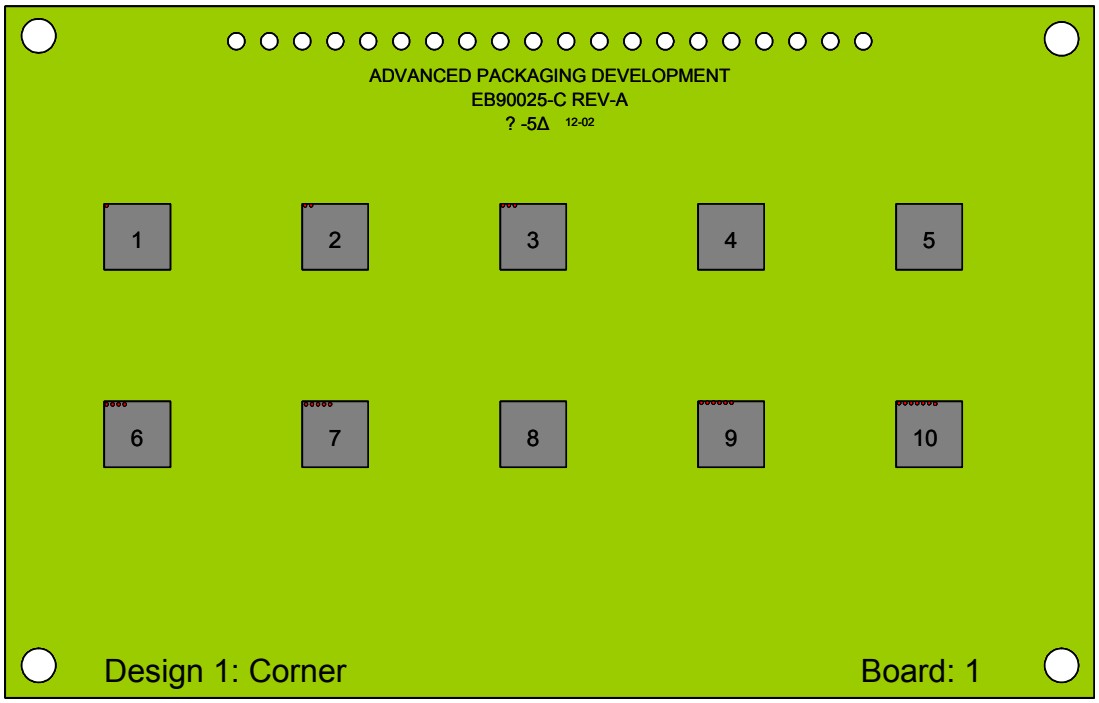


Figure 4-6: PCB Design with Open Bumps Starting from a Corner (Design 1).

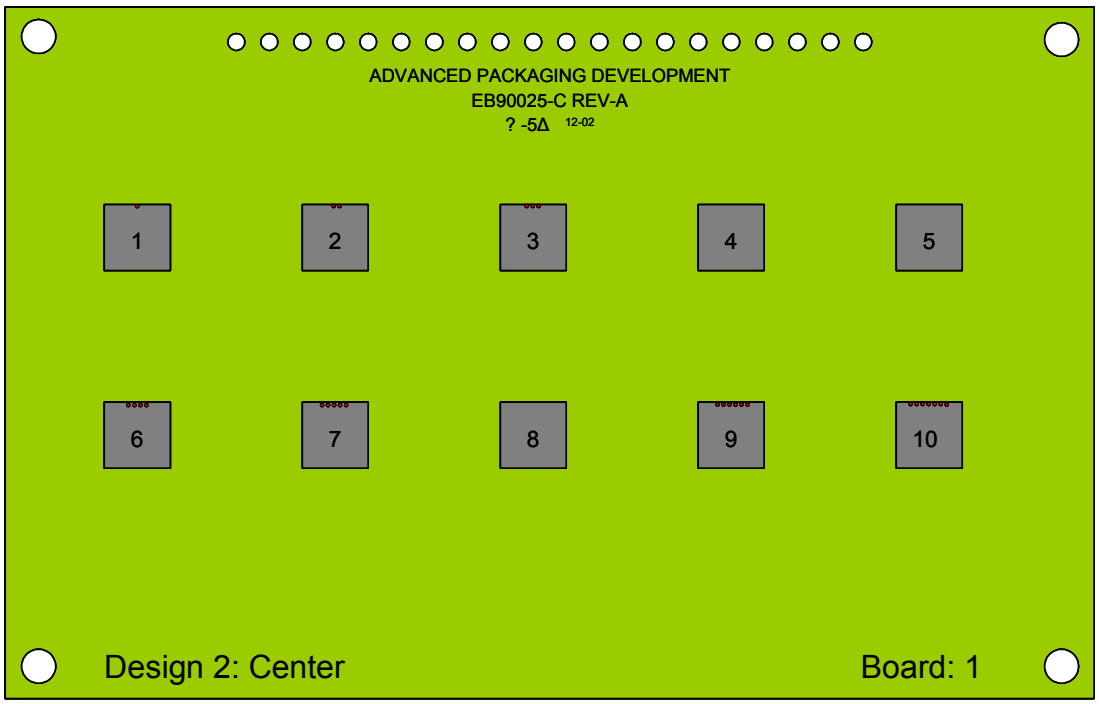


Figure 4-7: PCB Design with Open Bumps Starting from the Middle of a Side (Design 2)

Figure 4-8 presents a summary of the location and severity of defects. Each row of the figure represents a single row of twelve solder bumps on one side of a different chip, and the white circles indicate the location of the open solder bumps. The open bumps in the middle of a side were added in sequence to keep the pattern of open bumps centered. Seven defective devices from one series, corner or middle opens, are placed on one board along with reference chips with no open bumps.

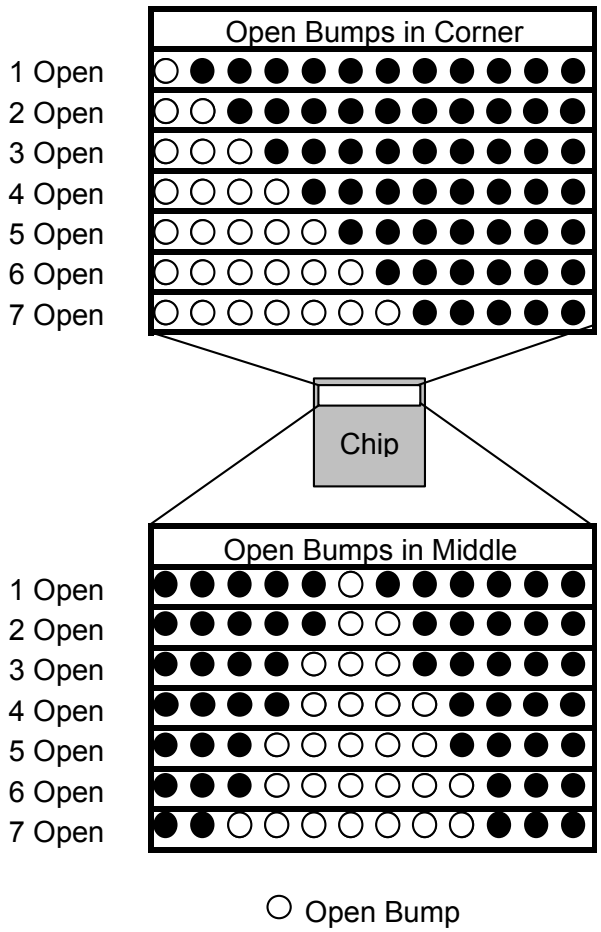


Figure 4-8: Schematic of Location of Open Solder Bumps

4.4.1 Circuit Board Assembly

To recreate the actual manufacturing process, the test die and the modified circuit boards were shipped to Solectron, Inc. in Charlotte, NC for assembly. The facility is an active manufacturing facility, and the test samples were assembled under standard manufacturing conditions. The parts were loaded into a pick-and-place machine that dipped the chips into a 1.5 mil thick layer of Kester 6522 no-clean flux before placing the chips in the positions on the PCB. A standard eutectic reflow profile was performed in a nitrogen atmosphere. Continuity for each chip was checked immediately after the parts exited the reflow oven.

The boards were marked with serial numbers using an etching system before the chips were attached to the board. The bottom edge of each board bears the designation of "Design 1: Corner" or "Design 2: Middle" to indicate whether the open bumps are in the center or the corner of the chips.

4.4.2 Verification

To verify that the correct number of open joints was created on each sample, an electrical continuity check was performed. Each of the chips has electrical opens only where they are planned. Therefore, the build was successful in creating the defects that were desired. However, verifying the mechanical open condition was more difficult.

Even though all of the samples checked out electrically, the other goal for the build was to create a mechanical open. In order to verify that an air gap exists between the defective bumps and the PCB, two methods were attempted. X-ray and scanning

acoustic microscopy were implemented. Although these methods are known to have difficulty with this kind of inspection, no other non-destructive options were available. A destructive evaluation after the testing is complete would not even be a viable option, as the curing of the epoxy used to mount the specimens may either increase or decrease the gap between the bump and the board.

Figure 4-9 shows an x-ray image of the solder bumps on a chip with intentionally created defects. The image was taken with a Fein Focus x-ray system, having the ability to rotate the specimen nearly ± 90 degrees. The picture was taken at an extreme angle close to 90 degrees in order to capture the profile of the solder bumps on Design 2 Chip1 (one open bump in the middle of a side). However, no visible difference is seen between the properly connected bumps and the open bumps, and a white line on the picture shows that the bottom of the bumps is approximately the same across the entire side. The main difference is the absence of the metal solder pad under the bump, verifying that enough material was removed to completely delete the solder pad.

Figure 4-10 shows an image collected from an ultrasonic C-scan of Design 2 Chip 10 (7 open bumps in the middle of a side). The scan was performed with a 230 MHz focused transducer, and the spatial resolution for the raster scan was set at less than 10 microns. No change is observed between the properly connected bumps and the open bumps. Therefore, the same amount of energy is being transmitted through the bumps or reflected from the interface between bump and the board. Although the bumps next to the open bumps look different, they are electrically connected. Therefore, the problem must lie with the ultrasonic imaging for those three bumps.

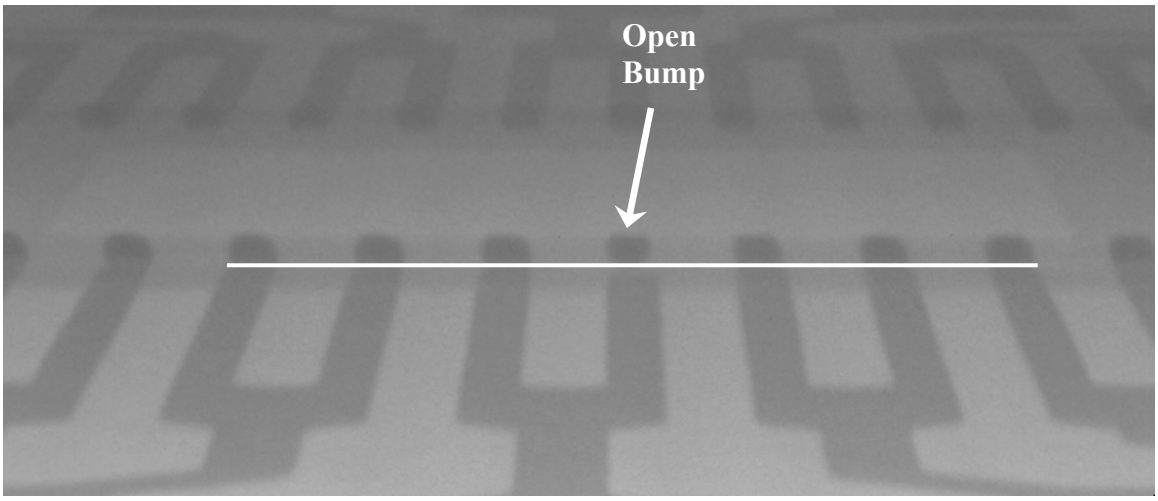


Figure 4-9: X-ray Image of an Intentionally Open Solder Bump

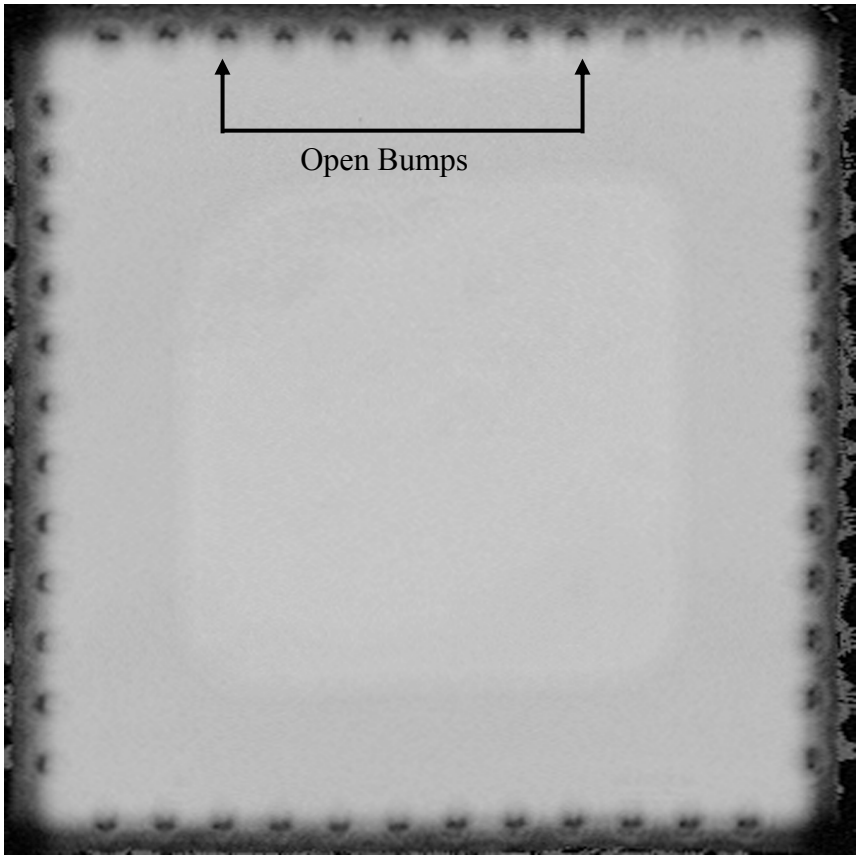


Figure 4-10: C-SAM Image of Open Solder Bumps

Since these are the only analysis tools available, the conclusion that can be drawn is that the bumps are most likely making contact with the board. This result is not entirely unexplainable. Manufacturing engineers rely on the surface tension of the solder bumps to be strong enough to "self-align" the chip with the solder pads during the reflow process. Therefore, the good solder bumps may pull the intentionally open bumps into contact with the PCB board, even though the solder pad is missing. For the purposes of the experiment, the samples represent an actual condition from the manufacturing process, so the results are relevant to the type of response that can be expected from a naturally-occurring defect of this type.

The samples constructed using this method were used for the repeatability and sensitivity experiments, as well as the modal parameter investigation. Results using these samples are presented in Chapter VI (Sensitivity) and Chapter VII (Modal Parameters).

4.5 Data Collection Procedure

The data collection procedure requires synchronization between the generation, detection and motion systems. Before data was taken, a study was made of possible experimental errors. Details of the setup and calibration are presented in the following sections.

To obtain vibration signals from the specimens, the laser ultrasonic method was used. The chips were excited into vibration using the pulsed Nd:YAG laser to irradiate the surface of the specimens. Laser pulses were delivered through a fused silica optical fiber with a 400 μm core diameter. Focusing optics were used on both the coupling and the distal end of the fiber, preventing dispersion of the laser pulses and providing the most

efficient coupling between the laser source and the specimen. Therefore, the focusing objective was adjusted to produce a laser spot of about 500 μm in diameter was the source of insonification, as shown in Figure 4-11.

The laser pulses were aligned with the center of the specimens, and the inspection points were located at ½ the solder bump pitch away from the solder bumps toward the center of the chip. A total of 48 inspection points were used, and the points were located at the mid-point between two adjacent solder bumps.

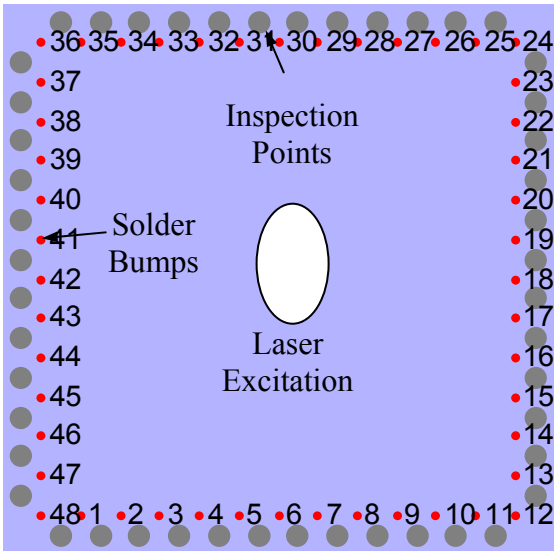


Figure 4-11: Flip Chip Inspection Locations

Although the geometry of the solder bumps is symmetric, the vibration response from different inspection points is not identical. Symmetrically located points have similar responses, but there is not a good way to identify the correct inspection location without taking all of the data. The main goal is to compare the signals at a given

inspection point from one chip to the next, looking for significant changes. Changes in the signal indicate defects in the area near the inspection point. Therefore, it is very important to get a good reference to compare with all of the other chips.

The interferometer measurement records the displacement of a point in time, which was caused by the vibration induced by ultrasonic generation. Enough acoustic energy must be created to cause the entire chip to vibrate. Therefore, the laser provided pulses with an average power of 50 mW, duration of 6 ns, and the pulses occurred at a frequency of 20Hz, allowing plenty of time for the chip to settle down before the next pulse arrived. After the chip starts to vibrate, the natural vibration dissipates over time, as the displacement of the surface is recorded. Signals were acquired with an automated data acquisition system, using a sample frequency of 25 MHz with 12-bit resolution, which is fast enough to capture the vibration signals in the 50 kHz to 2 MHz range. The trigger for the laser Q-switch was used to trigger data acquisition, and the signal was averaged multiple times, from 16 to as many as 128 times, at each point to eliminate high-amplitude random white noise, improving the signal-to-noise ratio.

The final step was to correctly align the interferometer at the inspection points. For this step, the positions of the inspection points were calculated from the manufacturer's documentation, and the automatic scanning routine in the data acquisition program was run to record the data. Data files were saved and stored for off-line processing to allow new algorithms to be tested, however, once a final analysis procedure is established, the data analysis can take place in real-time. Details of the data analysis procedures are reserved for discussion with the presentation of the data.

CHAPTER V

FLIP CHIP RESULTS

Multiple experiments were performed on flip chip samples with intentionally created open solder bumps. All of these samples are from the first set of experimental samples, however, the data indicates that the assumptions about modal vibration responses being initiated are correct. In addition, several potential sources of error were investigated. Each of these sources was either shown to not be a critical source of error, or a countermeasure was developed to prevent that source from appearing in the sensitivity analysis. These samples are representative of one type of typical manufacturing defects, and the results show the consistency and sensitivity of the inspection procedure.

5.1 Potential Sources of Error

Several potential sources of error in the procedure were identified. Simple tests were performed to measure the effect that each source has on the overall testing method, and the results are presented here. A few of the variables which affect the performance of the system are signal noise level, inspection location, misalignment of the excitation laser, and misalignment of the measurement laser. Howard (2002) has previously measured the misalignment and fixture stability variables. The design of the system is

robust, preventing misalignment of the lasers with the test specimens. Therefore, only the signal noise level for this flip chip and the relation between vibration responses on the top of the chip to a vibration response on the board adjacent to the chip are presented.

5.1.1 Signal Noise Level

Because of the opportunity to obscure meaningful data, the signal noise level is very important to establish. In addition to the noise obscuring the data, the risk of a systematic electronic noise appearing as data is also very real. Therefore, specimens were put on a circuit board, and baseline data was taken with and without the laser excitation laser being turned on. Of particular interest was the presence of high-frequency noise or high frequency signals that are not related to the behavior of the chip's response. A plot of the 1.0-2.0 MHz bandwidth limited FFT of the system noise and the vibration response signal are shown in Figures 5-1 and 5-2. The FFT of the system noise has no inconsistencies at a specific frequency that may distort the vibration responses measured from experimental samples. The noise is broadband, white noise, and it can be reduced through signal averaging.

In comparison to the noise measurement, the signal in the 1-2 MHz frequency range is on the order of 20 dB stronger than the noise measurement without a signal. Clearly, the signal is well above the noise level for the system. Because there are no discernable signals in the background noise, the confidence in experimental results can be very high.

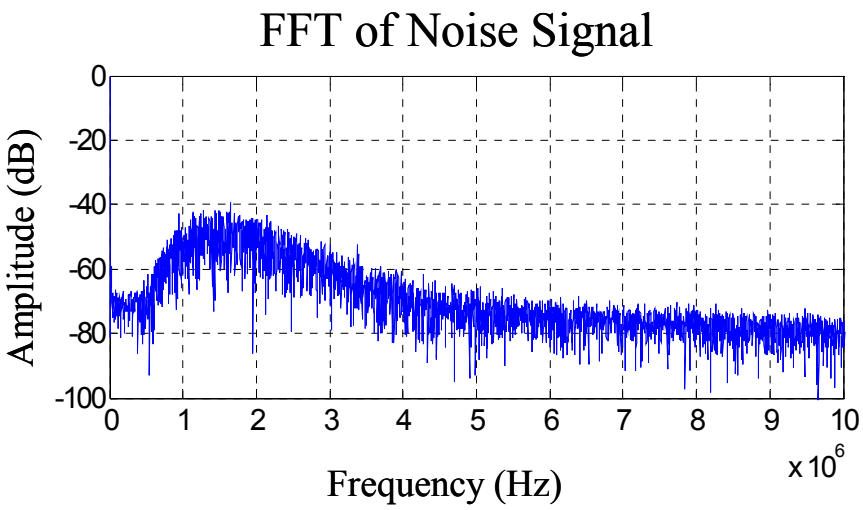


Figure 5-1: 1.0MHz to 2.0 MHz Digitizer Signal with No Flashlamp Pulse

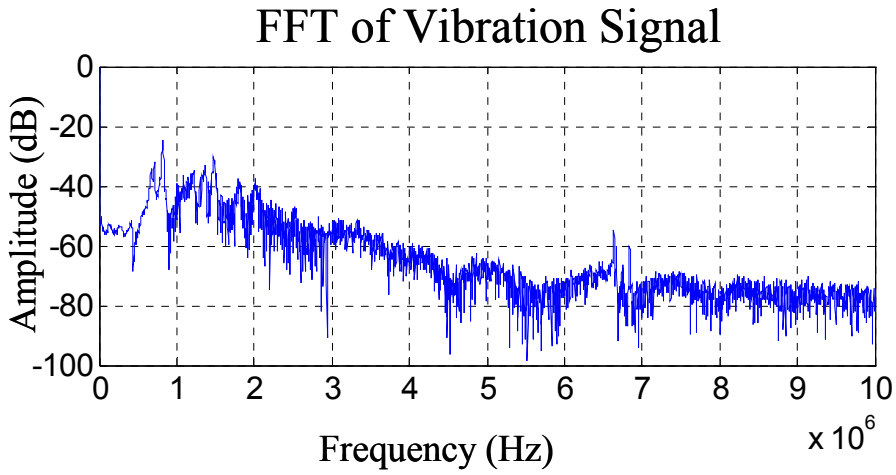


Figure 5-2: 1.0 MHz to 2.0 MHz Signal From Flip Chip Surface

5.1.2 Comparison of Bump to Board Signals

A possibility exists for transmission of the vibration response through the bumps to the surface of the circuit board. Therefore, an experiment was performed to test the

difference in the signals directly before and after a solder bump may have interacted with the acoustic wave. Data was taken directly above the position of the bumps under the chip and at a position on the trace leading to the bumps, as close to the chip as possible. The layout of inspection points are shown in Figure 5-3.

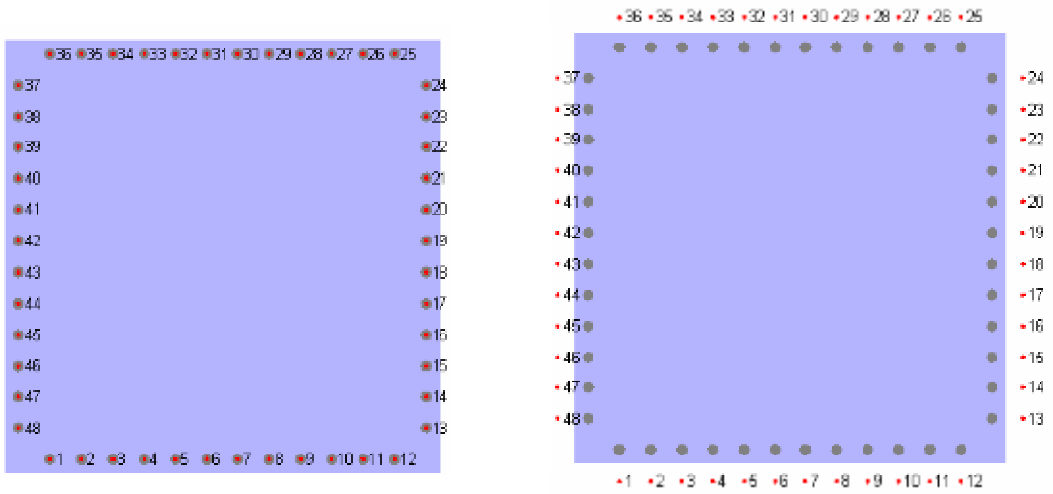


Figure 5-3: Inspection Points for On-Bump to On-Board Comparison

First, a visual comparison of the time-domain response provided a good first look at the signal. Therefore, the signal at a corner position for a chip with four adjacent defects at the corner is presented in Figure 5-4. The two signals look very dissimilar, and the amplitude for the signal on the chip is much higher than the signal on the board, which is to be expected, as not much acoustic energy can be transmitted by the solder bump. However, the board had a constant vibration that the signal from the chip settles down to match.

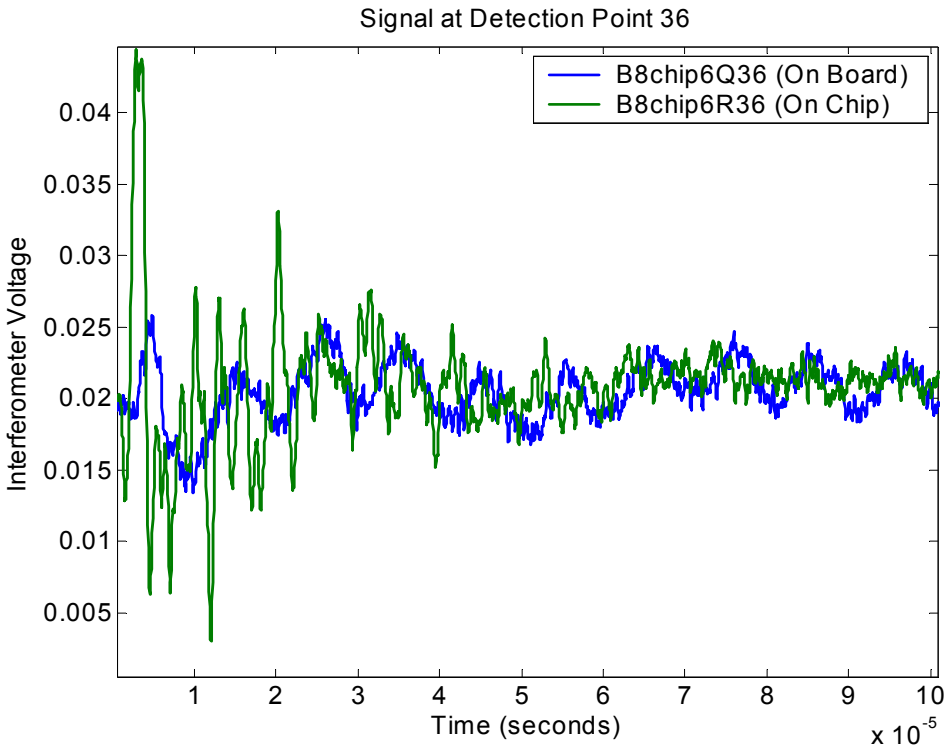


Figure 5-4: Comparison of Vibration Signal Before and After Passing Through a Solder Bump

An FFT was taken of the vibration response signals from Figure 5-4 and from the vibration response recorded from a reference chip at the same positions on and off the board. The normalized power is plotted in Figure 5-5, and it shows that the vibration from on top of the chip has a much more diverse frequency content than the vibration response from the board. In addition, the signals from the two chips, one reference and one with four open bumps at the inspection location, compare with each other much more consistently than with the signals from on the board.

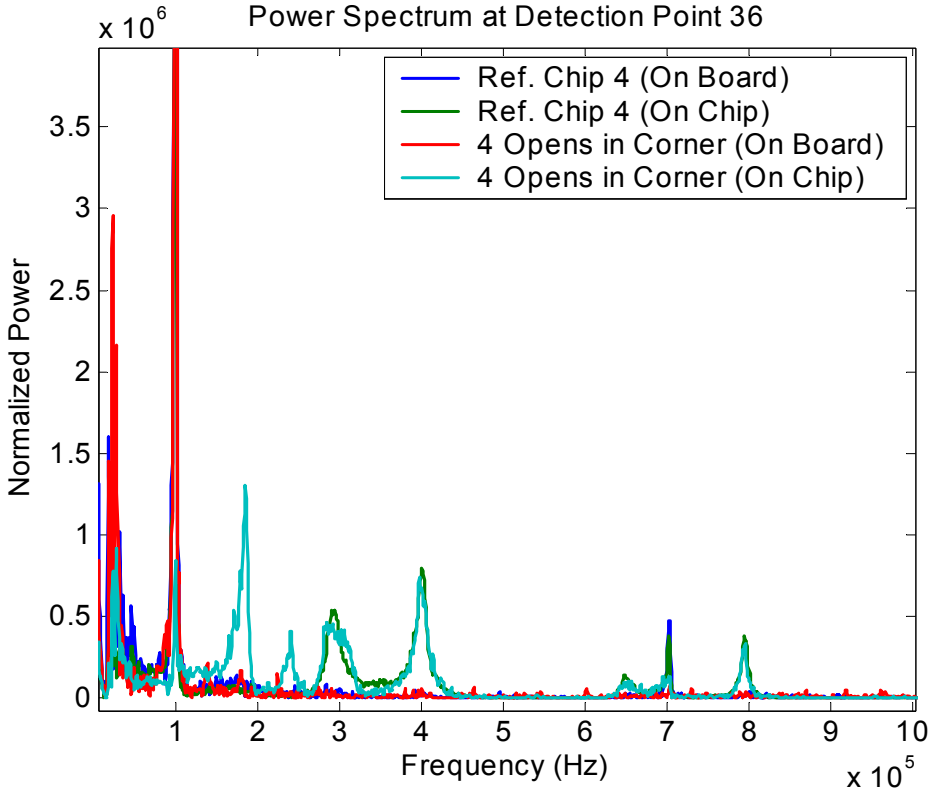


Figure 5-5: Comparison of Vibration Signal Before and After Passing Through a Solder Bump

The final test is to apply the Error Ratio method of comparing the signals. The ER plots for the chips that were measured are shown in Figures 5-6 through 5-9. A total of four plots are shown, and the first two represent data taken on the surface of the chip. The difference in ER values between Figure 5-6 and Figure 5-7 is caused by the presence of four open solder bumps at that corner of the chip. The same difference is present between Figure 5-8 and Figure 5-9, however, the signal to noise ratio between reference chips compared to each other and a reference chip compared with the chip having four open bumps in the corner is not as large. Therefore, measuring vibration response data

on the surface of the board is possible, but it is not as sensitive as the vibration response data from the top surface of the chip. The vibration responses recorded from the top surface of the chip have a much broader frequency spectrum, which may help in determining the presence of open solder bumps.

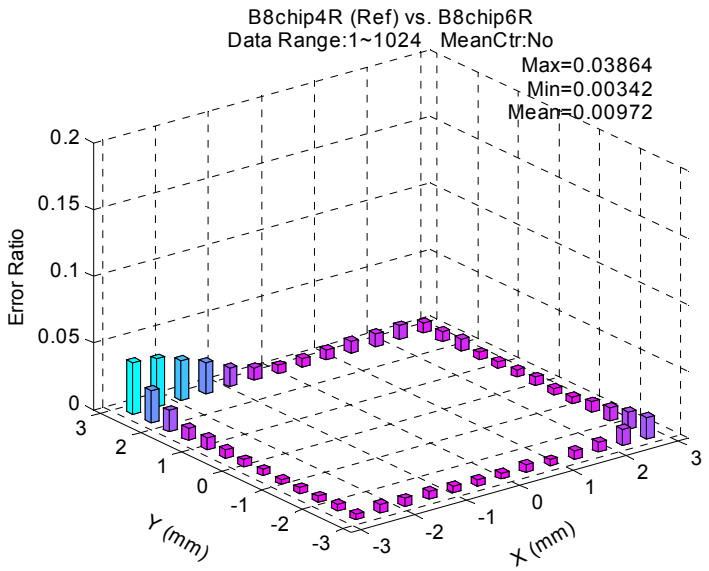


Figure 5-6: Error Ratio Values Directly Above Each Solder Bump, Reference Chip Compared with Chip Having Four Defects in a Corner

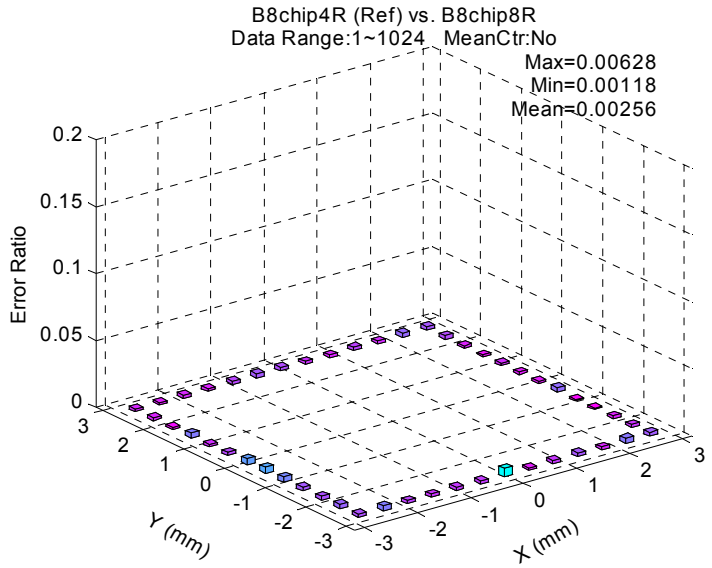


Figure 5-7: Error Ratio Values Directly Above Each Solder Bump, Reference Chip Compared with 2nd Reference Chip

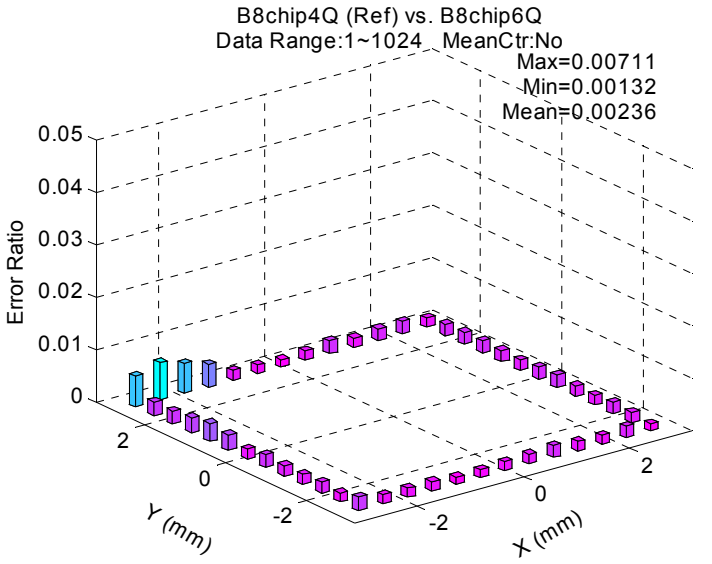


Figure 5-8: Error Ratio Values Directly Adjacent to Each Solder Bump on the Board, Reference Chip Compared with Chip Having Four Defects in a Corner

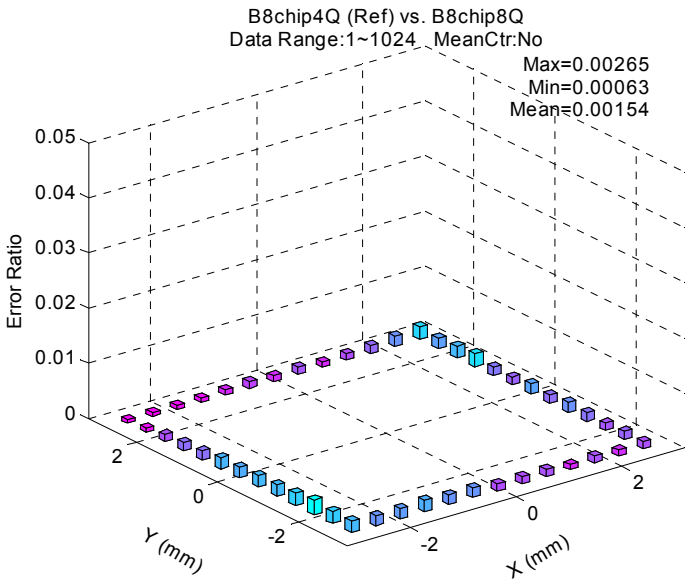


Figure 5-9: Error Ratio Values Directly Adjacent to Each Solder Bump on the Board, Reference Chip Compared with 2nd Reference Chip

5.1.3 Consideration of High-Frequency Response

Although the most easily excited and prominent modes of vibration are at lower frequencies, an examination of the vibration at higher frequencies was considered. Higher frequencies can be more sensitive to small changes than smaller frequencies because the wavelength is closer to the size of the changing geometry. However, these frequencies are also more subject to noise in the signal. From Figure 5-5, there are signals present at frequencies well above the 1-2 MHz range. The signals at high frequencies are shown to be much weaker than the signals at low frequencies. To identify the feasibility of evaluating high-frequency components of the vibration response, data was taken of the baseline noise in the system (laser power off) at the same

spot a signal was recorded. An FFT of a portion of the vibration response signal is presented with an FFT of the noise signal in Figure 5-10. The plot shows that the signal has a component at higher frequency, but it is relatively weak in comparison to the signal from the first several modes.

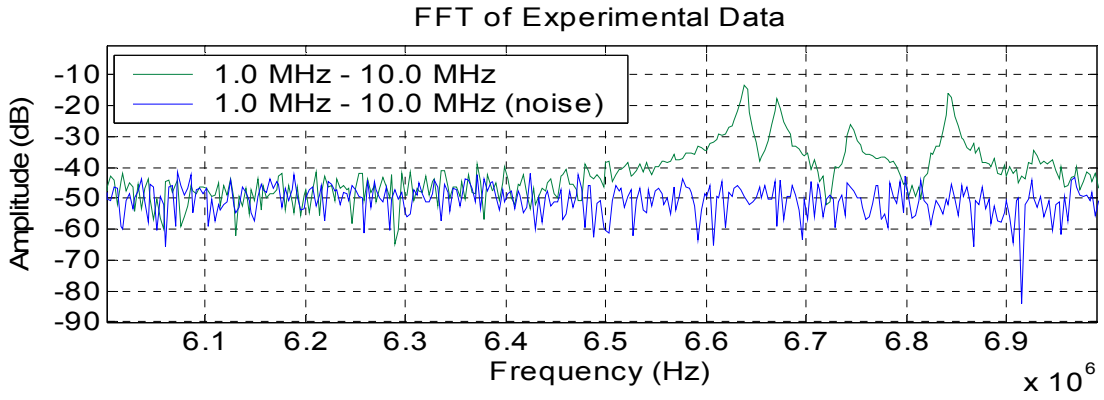


Figure 5-10: Signal to Noise Comparison in 6.0-7.0 MHz Frequency Range

In addition to the small signal strength, the high-frequency components are not always detected. Signals recorded near the corners of a chip contain more high-frequency components than signals recorded on other parts of the chip's surface. Even if the high-frequency signals can aid in detecting solder bump defects, the analysis would only be valid near the corners of a chip. These frequencies are also more susceptible to small errors in the geometry of the chip and errors in positioning.

5.2 Verification of Modal Vibration Behavior

Modal vibration behavior remains one underlying assumption to this research that remains to be tested, and this experiment will verify that full-field modal vibration is excited by the laser-generated ultrasound. Although the type of flip chip chosen for this

series of experiments only has 48 solder bumps, in order to test the full-field modal vibration profile, many more inspection points must be added. Therefore, a 13x13 array of points was created on the surface of the chip, as shown in Figure 5-11. Data was collected at each point, while the laser excitation spot was held fixed at the center of the chip with an incident power of 50 mW. The sampling rate was 25 MHz, with 12-bit resolution and 128 signal averages that reduced random white noise. Data was taken on reference chips, as well as chips with one to three adjacent open solder bumps in the corner and in the middle of a side. Location of the open solder bumps is identified in Figure 5-11.

Figure 5-11: Inspection Point Location for Modal Vibration Verification Test

5.3 Mode Separation Analysis

After collecting the data for 169 inspection points on each chip, the data was analyzed to show that individual modes could be isolated from the time-domain vibration response. An FFT was taken of the time-domain data and peaks from the FFT were used to define ranges for passband filters which were applied to the data. By carefully selecting a narrow passband, the time-domain response shows a single mode of vibration. Several modes were identified, and plots showing the surface displacement measured as a snapshot of the modal vibration are plotted in Figures 5-12 through 5-15. Not all of the modes are plotted, but these plots show representative modes of the chips' surface responses. The full range of modes detected was between 100 kHz and 1.4 MHz, so a broad range of identifiable vibration modes are present.

The full-field test of the flip chip specimens confirms that multiple vibration modes are excited using the laser-generated ultrasonic method. Identifying the modes and determining their shape is only the first step, however, because the stability, repeatability and sensitivity to defects still remain to be established. The next chapter explains in detail a controlled experiment that allows for the establishment of a measurement limit, based on the repeatability and consistency of the Error Ratio values. Chapter VII explains the analysis of the same data using the modal properties.

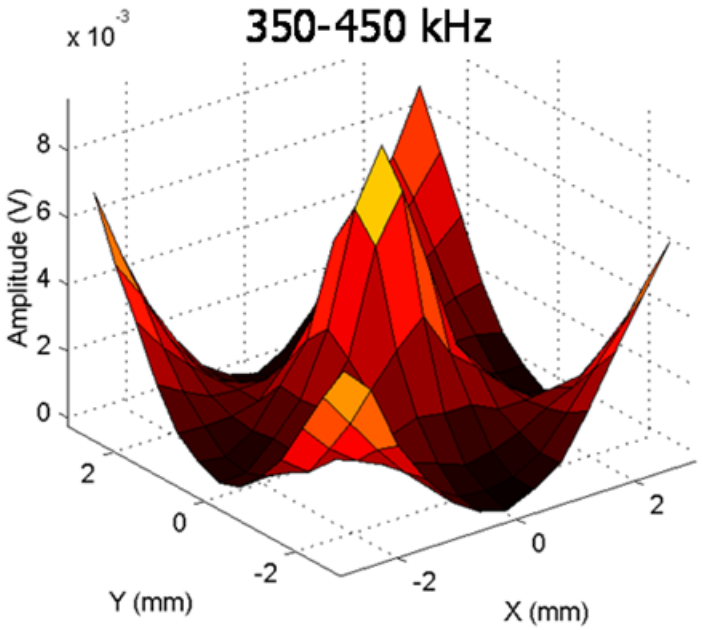


Figure 5-12: Vibration Mode Shape in 350 kHz- 450 kHz Passband on Surface of Chip

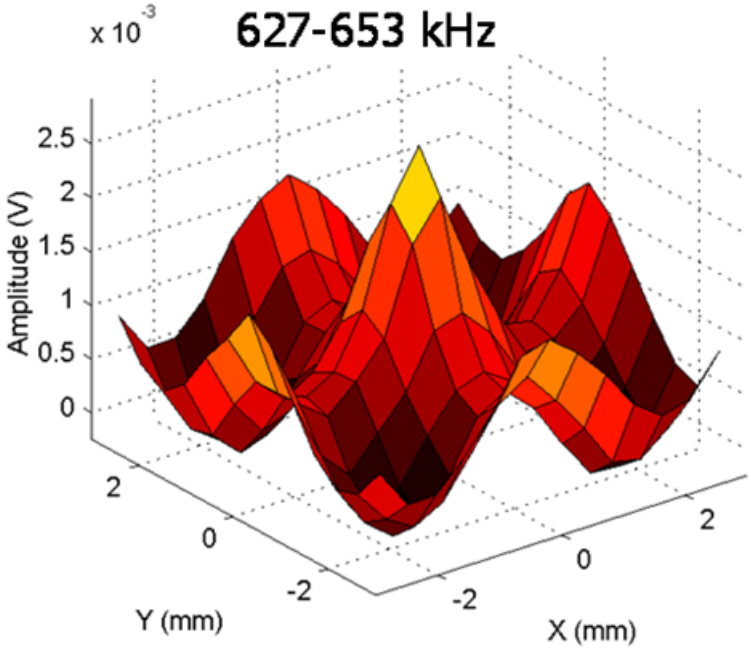


Figure 5-13: Vibration Mode Shape in 627 kHz- 653 kHz Passband on Surface of Chip

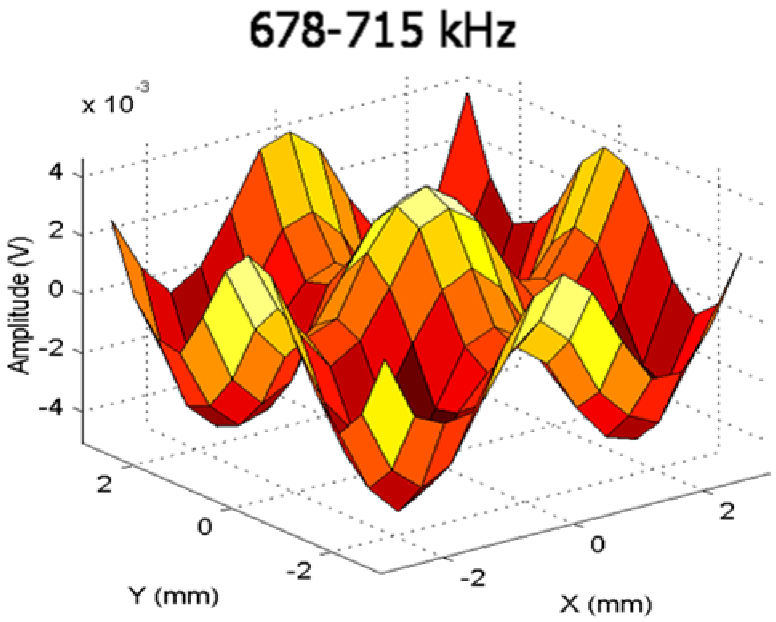


Figure 5-14: Vibration Mode Shape in 678 kHz- 715 kHz Passband on Surface of Chip

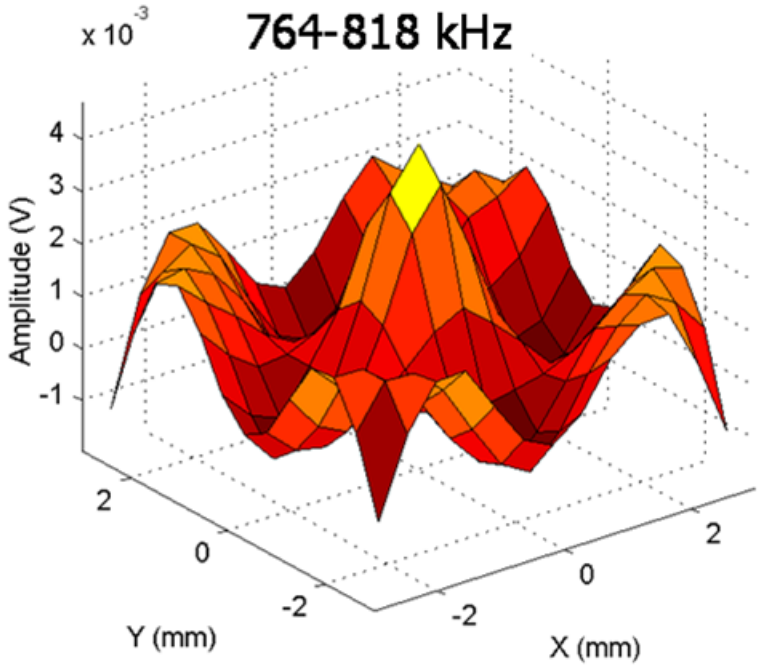


Figure 5-15: Vibration Mode Shape in 764 kHz- 818 kHz Passband on Surface of Chip

CHAPTER VI

FLIP CHIP ERROR RATIO MEASURMENT LIMIT ANALYSIS

Although previous work has successfully identified missing solder bumps on flip chip and CSP packages, missing solder bumps are a relatively rare occurrence in a manufacturing environment, as the flip chips and CSPs are inspected for all their bumps just before they are placed on the PWB (Liu, 2000), (Howard, 2002), (Erdahl, 2000). However, open solder joint conditions do occur more frequently, and this work tests the resolution of the laser ultrasonic system for identifying open solder bumps on flip chips, using flip chip specimens with intentionally created defective solder bumps.

To determine the ability of the current inspection system to identify open solder joints, the peripheral array, 48-bump daisy-chain device (PB-18) was mounted on the PWB without underfill by Solectron, as described in Chapter IV (Erdahl and Ume, 2005). The device has a higher I/O count and smaller, more closely spaced bumps than previous flip chip specimens. Individual solder pads were removed from the PWB design, and test specimens with zero to seven adjacent open solder bumps were created. Exciting the chips with laser pulses, the impulse responses at 48 points on the surface of each chip were recorded. Data analysis is performed to compare the responses from reference devices and devices with open solder joints. Results show that the system has the ability to detect open joints for the flip chip package, and statistical analysis of the calculated comparisons is employed to establish a detection threshold (Erdahl and Ume, 2005).

6.1 Experimental Setup

The experimental setup for this experiment is fully described in Chapter IV. The excitation laser is incident on the flip chip in the center of the chip, and 48 inspection points were recorded for each of the chips, in the pattern presented in Figure 4-11.

To minimize data acquisition errors, experimental procedures are carefully controlled. The Nd:YAG laser is allowed to warm up, providing a stable power output for the infrared excitation pulses, and the interferometer requires a warm up period to minimize noise in the detection measurements. While warm-up occurs, a PWB is loaded on the stage and the output from the vision system is verified, allowing calculation of the location of the flip chip samples on the stage. The excitation laser and interferometer are aligned to the flip chip, and the excitation laser is pulsed at 20 Hz, while the vibration responses are recorded at 25 MHz with 12-bit resolution.

6.2 Time Domain Vibration Response

The time-domain responses, shown in Figure 6-1, provide a good comparison between the reference chip response and the response of chips with increasing number of defects near a single interferometer measurement point. Figure 6-1a shows the vibration response measured at inspection point 36, as shown in Figure 4-11, for chips with adjacent defects near a corner. Figure 6-1b shows the vibration responses recorded at inspection point 30, as shown in Figure 4-11, for chips with adjacent open joints in the middle of a side. An increase in the amplitude of the peaks and a small change in frequency are evident for both time-domain plots as the number of defects is increased. For chips with five adjacent open solder bumps, the waveforms are similar to the

vibration response from the reference (undamaged) chips. The responses from the reference chips are similar to each other, but the similarity between vibration responses from reference chips and defective chips makes the task of identifying defects more difficult.

6.3 Frequency Domain Vibration Response

A Fast Fourier Transform (FFT) was taken of the vibration responses shown in Figure 6-1a and 6-1b, to show the normalized power distribution in the frequency domain. As shown on the frequency domain plot, the fundamental vibration frequency is approximately 100 kHz, however there are a significant number of other frequency response peaks, but the amplitude of the peaks is significantly lower as the frequency increases to 1.0 MHz. For a small number of defects, the frequency of the response peaks does not change, however the distribution of energy between the different peaks does change.

The frequency response for Figure 6-2a is different from the response shown in Figure 6-2b. An explanation for this phenomenon lies with the natural vibration modes of the chip, which are tied to geometry. A corner has different boundary conditions from the solder bumps that are in the middle of a side. Therefore, the frequency distribution for each mode is different at each measurement point, as shown in Figure 6-2. Changing frequency content poses a problem for defect detection methods; however, positioning accuracy over every chip is within 5 μm, so the change in the frequency content is small from chip to chip, when comparing data at the same interferometer measurement point.

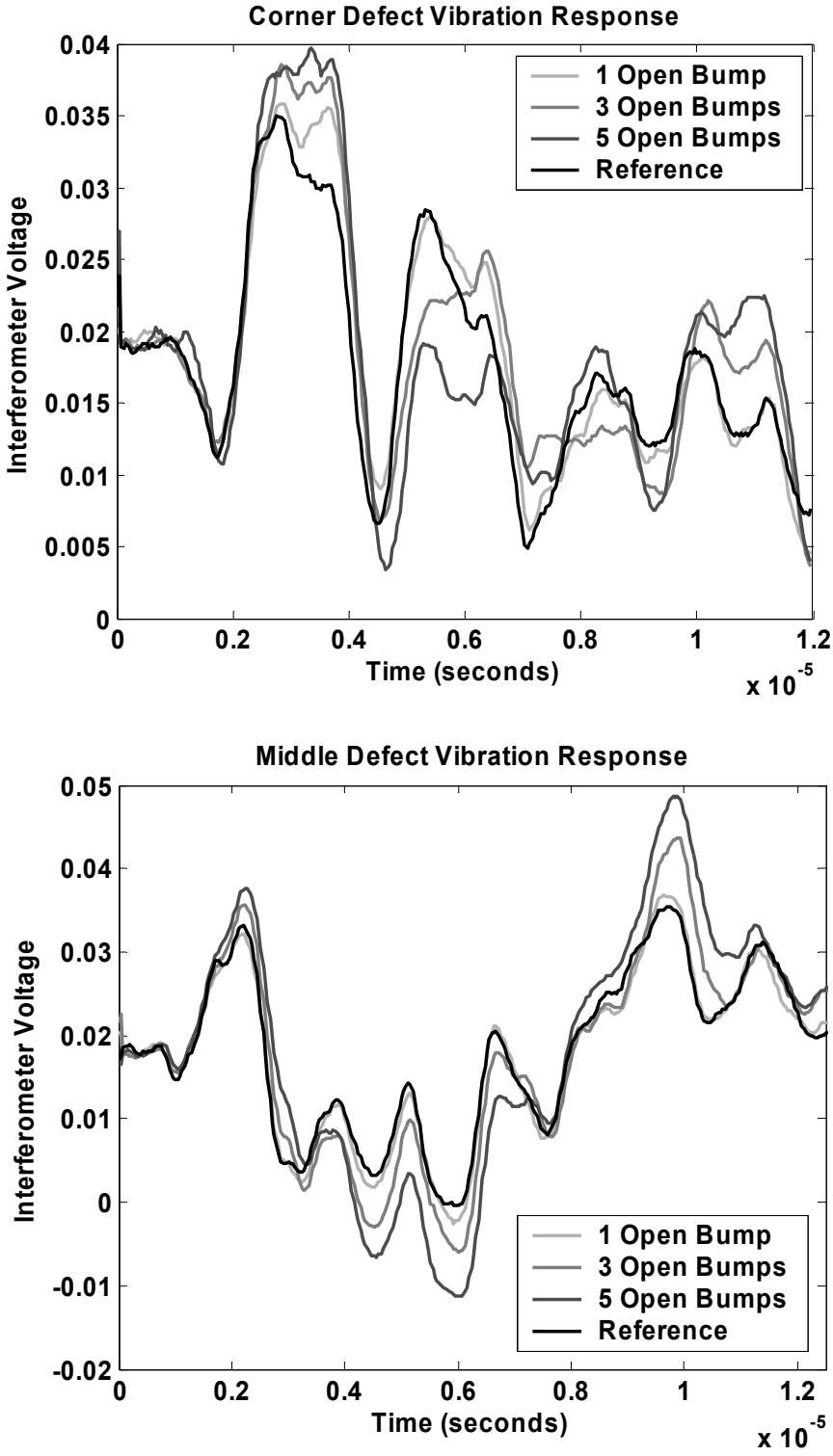


Figure 6-1: Time-Domain Vibration Response Changes at Defect Location a.) Defects in a Corner (pt. 36), b.) Defects in the Middle of a Side (pt. 30)

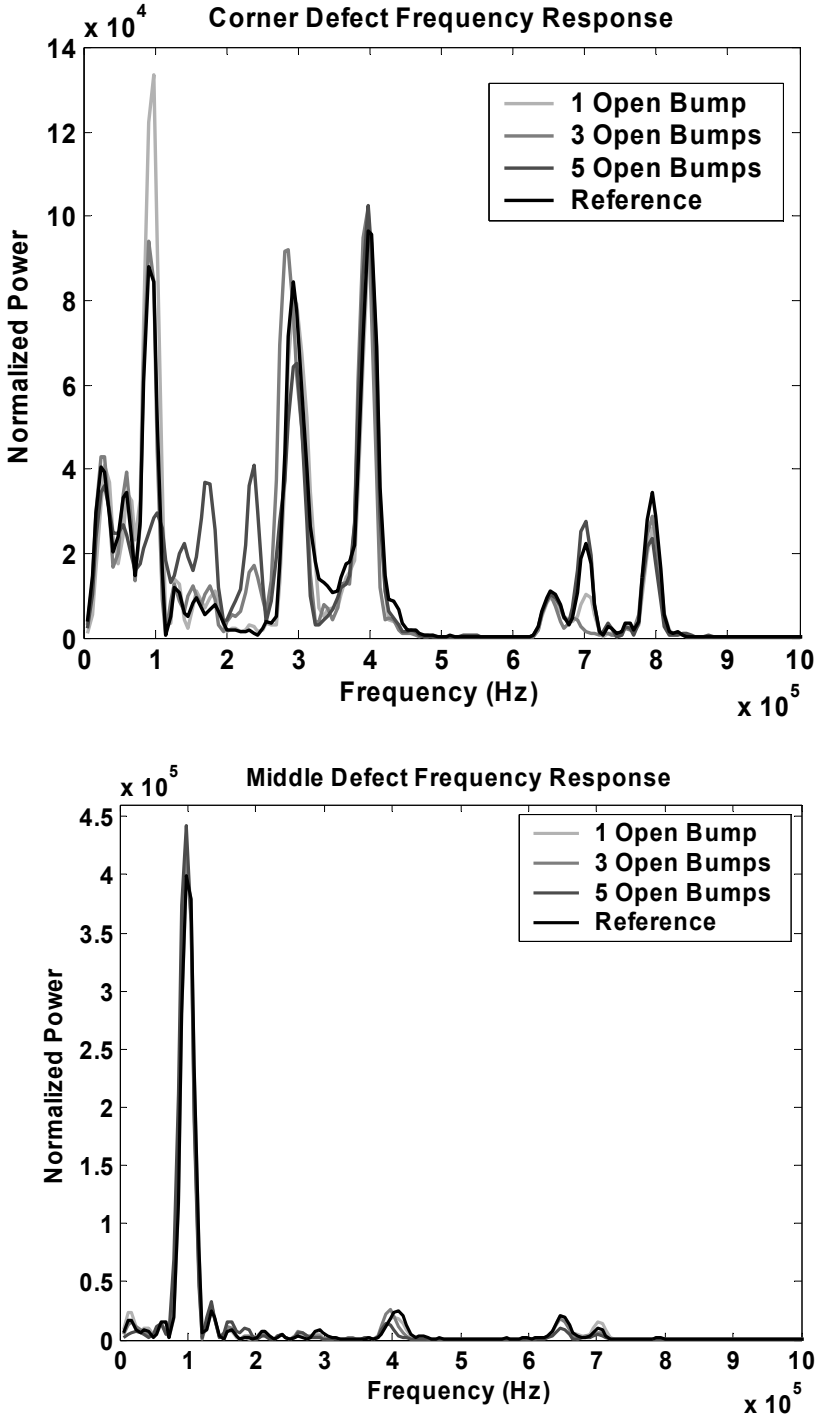


Figure 6-2: Frequency Domain Vibration Response Changes at Defect Location a.) Defects in the Corner of a Chip (Pt. 36), and b.) Defects in the Middle of a Side (Pt. 30)

Recorded vibration waveforms are compared with reference vibration waveforms through signal analysis methods both in the time and frequency domains. Pattern recognition systems have been used for other devices (Liu and Ume, 2002) (Liu and Ume, 2003), but straightforward comparisons are often enough to get good results, especially since only one type of defect is present.

6.4 Error Ratio Analysis

Measuring the changes in vibration responses between two flip chips is difficult to quantify directly because the signals closely resemble each other, but a signal analysis method has been previously developed for use with this system (Liu, Erdahl and Ume, 2001) (Liu and Ume, 2002). The Error Ratio (ER) is a simple comparison of the similarity between two waveforms. The total squared error between the two waveforms is normalized by the total squared area under one waveform, which is chosen as a reference, as shown in Equation 1:

$$\text{Error Ratio} = \frac{\int [f(t) - r(t)]^2 \, dt}{\int [r(t)]^2 \, dt}, \qquad (6\text{-}1)$$

where *f(t)* is the measured waveform, and *r(t)* is the reference waveform. If two vibration responses are identical, the error ratio value will be zero, but the value will always be positive when comparing any two non-identical waveforms. Since the value depends on the reference waveform, care must be taken to only compare very similar devices, and the devices used as a reference must be of relatively high quality. Changes in chip size, material properties, or placement on a board may cause significant changes in the value,

making this technique sensitive to all of these defects. However, the technique is also susceptible to measurement noise caused by acceptable manufacturing variation between specimens. To eliminate the measurement noise, a calibration study must be performed to determine the sensitivities to various defects for each new device being tested.

6.5 Error Ratio Results

To characterize the system resolution for open solder bumps, two sample boards, each having three reference chips and seven chips with intentionally created defects were tested. A total of 48 measurement points were recorded on each chip, following the inspection pattern in Figure 4-11. All ten chips on both boards were tested seven times to measure the consistency and repeatability of the measurement technique. The Error Ratio values were calculated for each of the chips, when compared to the rest of the chips on each board. Representative plots of the results are shown below.

Figure 6-3 shows the ER value calculated at each of the 48 interferometer measurement points. The same reference vibration responses were used to compare with the responses from the chips represented in Figures 6-1a and 6-2a with the time-domain and frequency domain responses. In comparison to the reference, the chips with intentionally created defects have a higher Error Ratio value close to the location of the defect in the upper left corner of the plot.

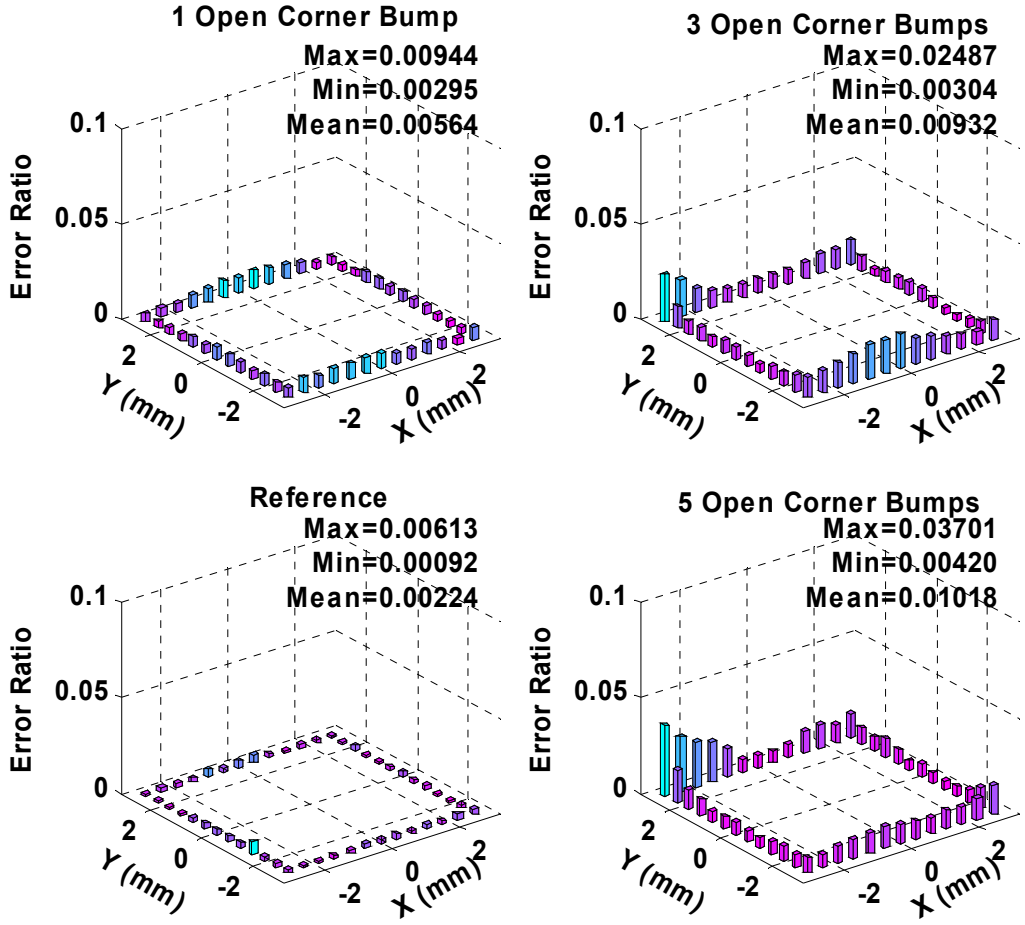


Figure 6-3: Error Ratio Values at Inspection Points for Chips with Defects in the Corner.

Figure 6-4 shows the ER values for selected chips from the second board, having intentionally created defects in the middle of one side of the sample chips. These are the same chips whose representative vibration responses are shown in Figures 6-1b and 6-2b. The location of the defect is shown by the maximum ER values, but the mean of all 48 values also shows the presence of defects, when compared to the mean value from the reference chips.

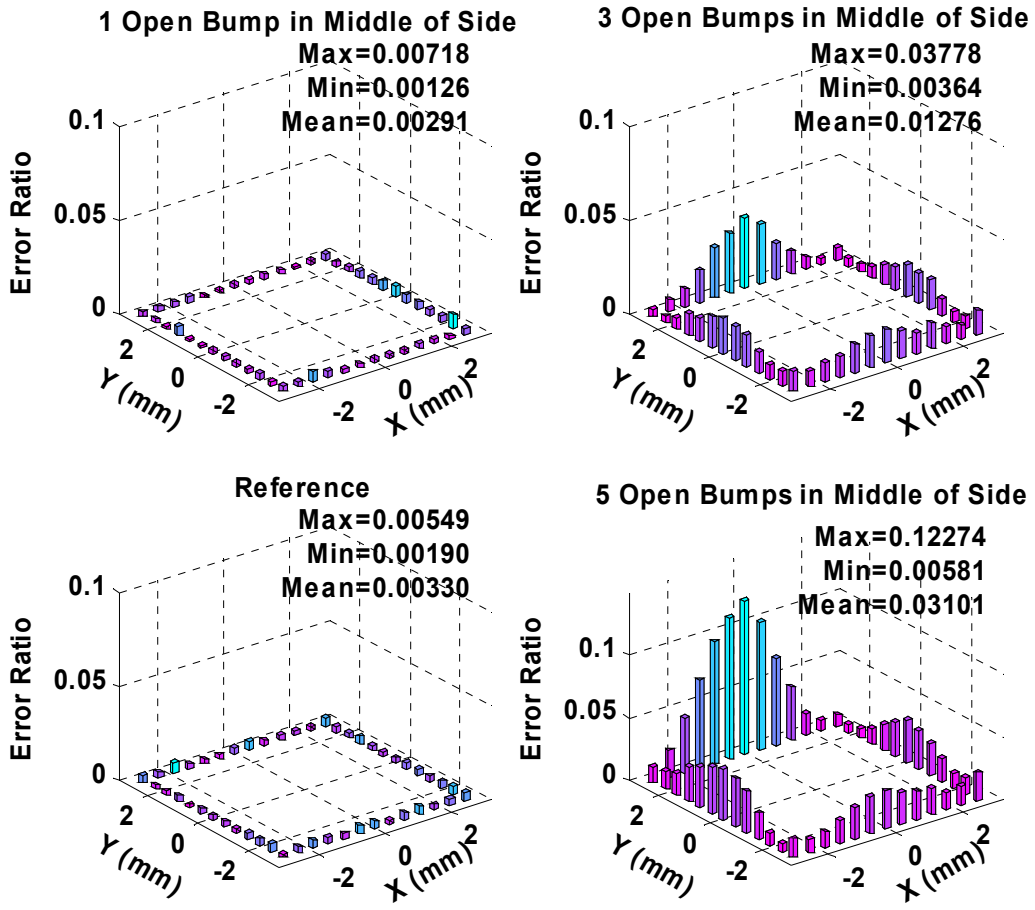


Figure 6-4: Error Ratio Values at Inspection Points for Chips with Open Defects in the Middle of a Side.

To condense the data from all the chips and trials, the maximum and the mean of all 48 ER values are used to discriminate between the reference and defective chips. The maximum and the mean ER values were calculated for each chip using two reference chips, and only data that was taken on the same trial were used to compute ER values. The seven sets of data, one from each trial, were averaged together, and the total values are presented in Tables 6-1 and 6-2. Because the reference chips are the only chips on each board that are identical, the reference chip ER values are averaged together to

establish the mean values and variability of the control group. The average maximum ER value and the average of the mean of 48 ER values, for each chip and trial, are presented with a positive two standard deviation value to establish a 95% confidence interval, that is a 95% likelihood that the results are correct. Only the positive values are shown because the ER values for defective chips are greater than for the reference chips. In order to detect an open solder bump defect, a threshold was set at the upper two-sigma value for the reference chips (Avg. +2σ),.as shown in Tables 6-1 and 6-2.

Table 6-1: Statistical Summary of Chips with Open Bumps in the Middle of a Side (7 Trials)

	48-Point Max. ER Value (7 Trials)		48-Point ER Mean (7 Trials)	
	Average	Avg. +2σ	Average	Avg. +2σ
Reference	0.0062	0.0088	0.0029	0.0043

	48-Point Max. ER Value (7 Trials)		48-Point ER Mean (7 Trials)	
	Average	Avg. -2σ	Average	Avg. -2σ
1 Open	0.0155	0.0076	0.0075	0.0041
2 Opens	0.0286	0.0174	0.0145	0.0037
3 Opens	0.0229	0.0159	0.0080	0.0066
4 Opens	0.0533	0.0350	0.0159	0.0086
5 Opens	0.0330	0.0240	0.0100	0.0073
6 Opens	0.0654	0.0408	0.0257	0.0176
7 Opens	0.2238	0.1357	0.0644	0.0387

Table 6-2: Statistical Summary of Chips with Open Bumps in the Corner (7 Trials)

	48-Point Max. ER Value (7 Trials)		48-Point ER Mean (7 Trials)	
	Average	Avg. +2σ	Average	Avg. +2σ
Reference	0.0064	0.0088	0.0033	0.0042

	48-Point Max. ER Value (7 Trials)		48-Point ER Mean (7 Trials)	
	Average	Avg. -2σ	Average	Avg. -2σ
1 Open	0.0100	0.0014	0.0040	0.0025
2 Opens	0.0110	0.0074	0.0052	0.0041
3 Opens	0.0371	0.0322	0.0135	0.0116
4 Opens	0.0473	0.0193	0.0215	0.0151
5 Opens	0.1176	0.1009	0.0318	0.0276
6 Opens	0.1415	0.1192	0.0395	0.0331
7 Opens	0.1001	0.0912	0.0350	0.0315

The data in Tables 6-1 and 6-2 show a significant difference between the average reference values, for the maximum ER value and the mean ER on each chip, and the average values for the defective chips. However, only the chips with three or more adjacent open bumps have -2σ values (Average-2σ) that are well above the threshold set by the reference chips. The chips with two adjacent open bumps have a lower limit that is close to the threshold, and the chance of both the maximum and mean value out of 48 inspection points being below the threshold is small. However, the -2σ values calculated for the chips with only one defect fall within the 95% confidence interval of the reference chips, making detection of chips with only one open bump difficult because some of the chips will have ER values that fall below the detection threshold.

Because the data for the chips with one open bump are inconclusive, the variance of the groups of data were analyzed to measure the significance of the difference between

the mean reference values and the mean values for chips with one open solder bump. The analysis of variance produces a measure of the statistical relationship between two means, and then the Student's t-test was employed to quantify the difference. With an t-value of 10.025, the changes in mean value were found to have a p-value of 0.008 (greater than 99.9% probability) when seven samples are taken. This significance decreases with a reduction in sample repetition. However, with only two sample repetitions, the t-test value is 21.6, indicating a p-value between 0.01 and 0.001. Therefore, detection of one open bump will require at least two repetitions of the testing procedure, using the current parameters, based on the current set of data.

6.6 Error Ratio Measurement Limit

Currently, the ER method of waveform comparison can detect two or more adjacent open bumps with a statistically significant probability of approximately 95% in a single test, since the -2σ values of the defective chips are greater than the upper bound on the reference ER values. However, an analysis of variance (ANOVA) indicates that the smaller change observed between the discriminating factors for the reference chip ER values and the chips with only one open bump is significant. Therefore, chips that have ER values close to the threshold value can be tested multiple times to ensure that the significant changes, correlated to bad parts, are identified. To improve the defect resolution, the variance of the reference group needs to be minimized, as a reduction in the standard deviation of the reference chips would improve the probability of detecting one or two adjacent open bumps. In order to reduce the variance of the reference group, the manufacturing processes may have to improve to remove any process-induced error.

CHAPTER VII

EXPERIMENTAL MODAL ANALYSIS

Although the ER method presented in Chapter VI does show sensitivity to open solder bumps between the flip chip package and the circuit board, one of the main goals of this research is to show the applicability of structural modal analysis to the problem of defect detection in electronic components. To accomplish this goal, the seven trials on each chip used in Chapter VI were re-analyzed using modal analysis methods. Similar results were achieved, but this direction does show promise for the application of structural modal analysis techniques to small structures.

7.1 Modal Analysis Process Overview

The modal analysis method utilized in this research is called the Algorithm of Mode Isolation (AMI), and it was developed by Ginsberg *et. al.* (2002). A composite fast Fourier transform (FFT) is created from data taken at several different locations on the surface of the chip. The FFT of each data sample is added together, and the resonant peaks on the FFT, each indicating a vibration mode (natural frequency), become more distinct. A curve is fit inside each peak, clearly defining the natural frequency of the peak and reducing the error in natural frequency estimation in spite of noise or closely spaced modes. Then, the fitted curve is subtracted from the composite FFT, leaving a

residual FFT that is analyzed as the next composite FFT (Drexel and Ginsberg, 2001). The process is repeated until all the strongly identified modes are extracted. Contributions from each mode are refined through and iterative procedure. Each mode is isolated in the system response, and then it is re-fit to obtain an improvement in estimations of its parameters. The results returned to the user include system properties such as the natural frequency, the damping ratio, and the mode shape of each vibration mode, which can be extracted from the FFT once the correct natural frequency is found. Changes in the natural frequency, damping ratio, or the mode shape all indicate changes to the system. For the purposes of testing devices using laser generated ultrasound, these changes are initially correlated to known defects, however, eventually the three metrics can be used in combination to identify unknown defects, such as open, missing, cracked, lean, or shorted solder bumps.

7.2 Linearity Check

Although the AMI method is robust for identifying modal properties from data that is contaminated by noise, a nonlinear vibration response from the flip chip package will distort the data from the real values. Therefore, an experiment was performed to determine if the flip chip has a nonlinear response for different laser excitation power levels.

The sample size was limited to three chips, two reference chips and one chip with four adjacent open bumps in the corner of the chip. The reference chips provide a baseline value, and the chip with four open bumps was chosen because the number of defects is in the middle of the range of defects being examined.

Each of the chips was inspected at three laser excitation power levels: 30 mW, 50 mW and 70 mW. This range of power levels brackets the typical laser power level used for inspection, so the effect of any nonlinearity can be determined at the operational point most commonly used. Data was recorded at all 48 inspection points that are used for all of the other experimental investigations.

To determine if a nonlinear vibration component is present, the data was processed using the AMI method. Two prominent vibration frequencies were extracted from the data, representing the modes that occur at 100 kHz and 800 kHz. Any shift in modal vibration frequency indicates a nonlinear response. Because there were seven trials available for the 50 mW power level, the values were averaged and a standard deviation was calculated for each mode. Table 7-1 presents the data extracted for this analysis on the three chips. Each value for frequency is in kHz and the 2σ value for the 50 mW level is provided as a reference for the level of experimental variability that occurs as a result of setup and noise.

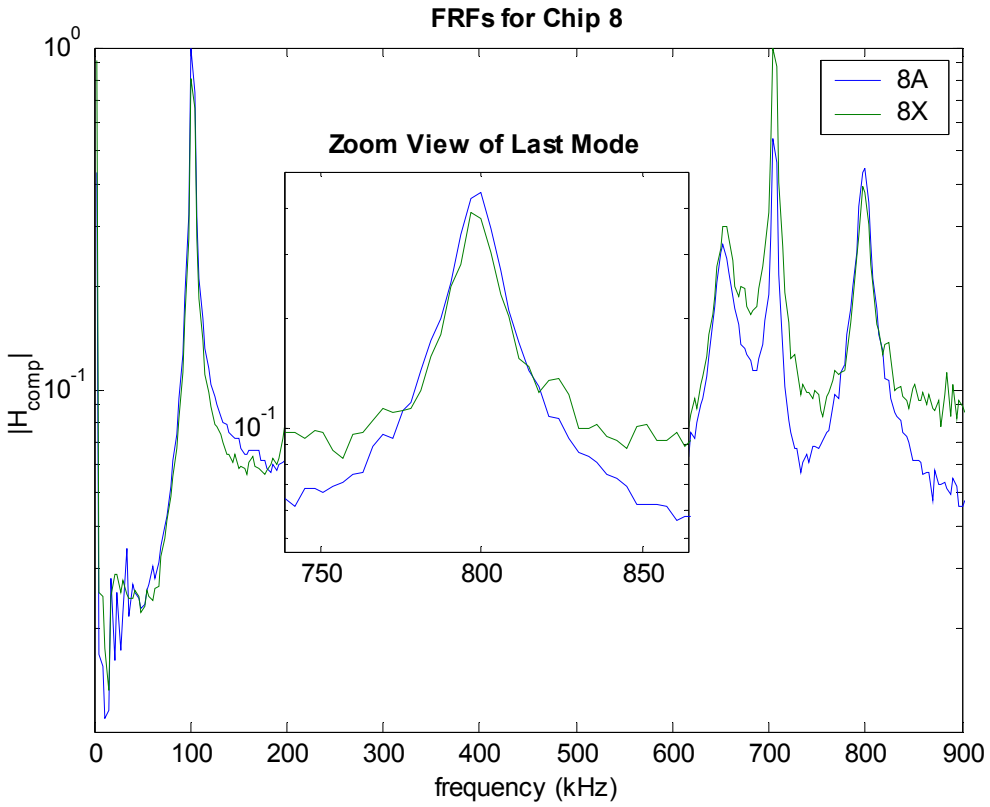
Table 7-1: Natural Vibration Frequencies at Three Power Levels

		Frequency (kHz)			
Reference Chip 1	**Power (mW)**		**2σ**		**2σ**
	30	101.94		799.14	
	50	101.9	0.086	798.42	0.133
	70	102.03		798.34	

		Frequency (kHz)			
Reference Chip 2	**Power (mW)**		**2σ**		**2σ**
	30	101.47		799.01	
	50	101.57	0.767	798.53	0.205
	70	101.61		798.58	

		Frequency (kHz)			
Chip with 4 Corner Defects	**Power (mW)**		**2σ**		**2σ**
	30	101.19		797.43	
	50	101.18	0.253	797.09	0.329
	70	101.28		797.13	

As shown in Table 7-1, there is not a significant shift in the two frequencies that were examined. The values are within the 2σ limit on the 50 mW data for the 100 kHz mode for each of the chips. For the 800 kHz mode, the 30 mW mode is outside the 2σ limit. To examine this effect, the composite FFT used to calculate the value for the 30 mW data is presented in Figure 7-1 with the composite FFT of one of the reference chips. A plot of the data shows a significant increase in the level of noise at the lowest power level, so the uncertainty in the data is much greater. The maximum shift in vibration frequency is about 0.7 kHz for the 800 kHz mode, and noise in the vibration response at lower power levels may cause this amount of shift.



7.3 AMI Modal Analysis Results

Although the Error Ratio method does successfully identify open solder bump defects, part of the goal of this work is to understand how the modal vibration properties change with the introduction of defects. Therefore, raw vibration response data from the repetitive trials on the flip chip specimens were subjected to analysis using the Algorithm for Modal Isolation (AMI). The natural frequency, damping ratio and mode shapes were extracted from the data for each of the trials, and the results are presented to classify the statistical significance of changes in these parameters. Although a majority of the effort

is focused on two prominent modes, the multiple-input, multiple-output (MIMO) version of the AMI algorithm could be used to more fully characterize the potential modes for this flip chip package. A multiple input inspection would require more than one excitation location, slowing down the inspection process. Therefore, it isn't as practical as the single-input, multiple output (SIMO) method.

7.3.1 Data Processing Procedure

Because of the time involved and the large quantity of data, the parameters that were investigated are limited. Only two very prominent modes from the data set were extracted using the SIMO version of the AMI algorithm. The mode selection was based on the amount of noise seen in the composite FFT plots for different chips and the consistent presence of these modes on every device that was tested. Depending on the setup, some of the less prominent closely spaced modes were not recorded for every chip or every trial on the same chip. However, some of the other closely spaced modes were observable when multiple drive points were used to excite the specimen. The remaining focus of the modal analysis will be on the 100 kHz and 800 kHz modes for the flip chip package.

The goals of this investigation are to identify the consistency and stability of these two modes (natural frequency, damping ratio, and mode shape) for seven experimental trials and to evaluate the potential for using these parameters to identify the presence of defects. In order to be useful detecting the presence of open solder bumps, the values for the reference chips (no open bumps) must be statistically different from the values for the chips with one to seven adjacent open solder bumps.

7.3.2 Single-Input Multi-Output (SIMO) Results

The natural frequency values for the 100 kHz and 800 kHz modes are presented in Figure 7-2. The seven trials for each chip are plotted together, and 2σ normal distribution curve is plotted directly above the data values, giving a direct way to check the statistical variation in the data values. Although the natural frequency values for both the 100 kHz and 800 kHz modes are tightly grouped, neither of the modes shows a strong correlation to the presence of open solder bumps. The change in the natural frequency for the 100 kHz mode can only be used to discriminate between reference chips and chips with three or more open solder bumps. The natural frequency extracted for the 800 kHz mode cannot be used to discriminate between reference chips and chips with open solder bumps.

Using the same format as in Figure 7-2, the damping ratio values are plotted for all ten chips and the seven trials on each chip for both board designs in Figure 7-3. The normal distribution is plotted over each set of trials on one chip. The values for the 100 kHz and the 800 kHz modes are consistent, but the distinction between the reference chips and the chips with intentionally open solder bumps is not clear. All of the chips have nearly the same overall damping ratio at 100 kHz, with a value of 0.01. For the 800 kHz mode, the damping ratio is approximately 0.006. Because the system has such a small level of damping, the changes caused by the presence of open solder bumps cannot be large. If the damping was high for a given mode, then the change in damping ratio should be more evident.

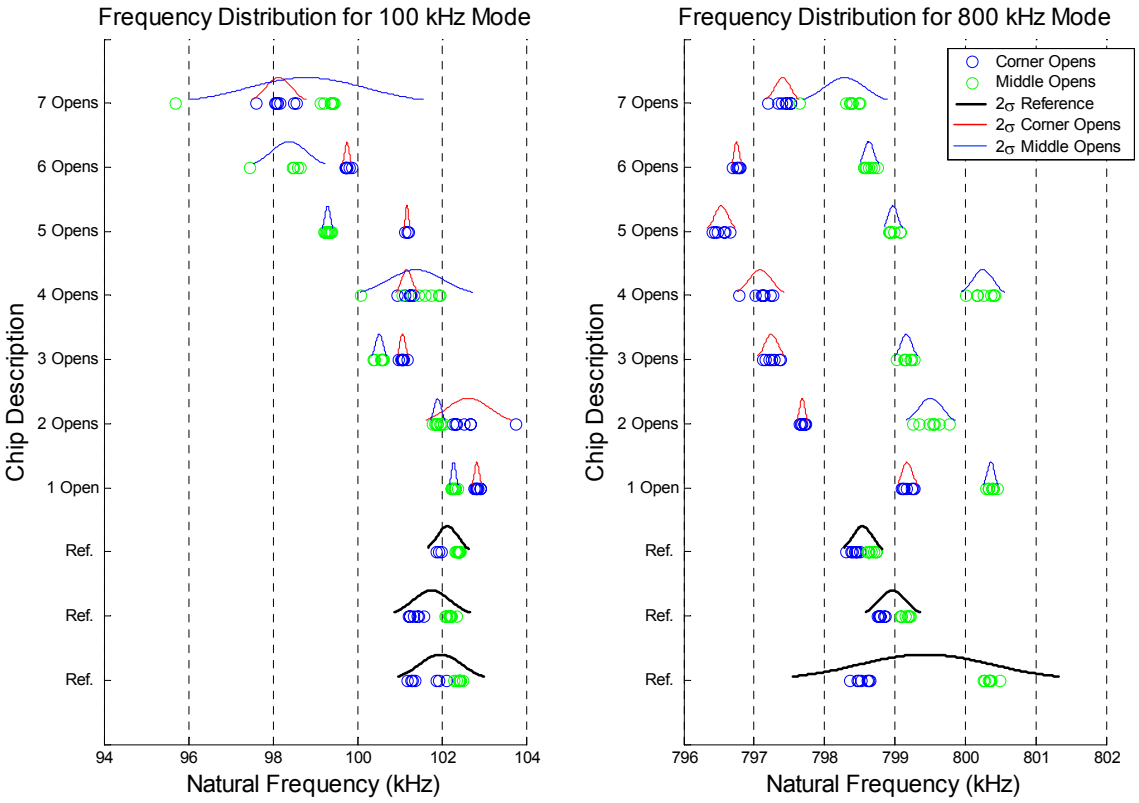


Figure 7-2: Natural Frequency Distribution for 100 kHz and 800 kHz Modes for 7 Trials on Board Designs 1 and 2.

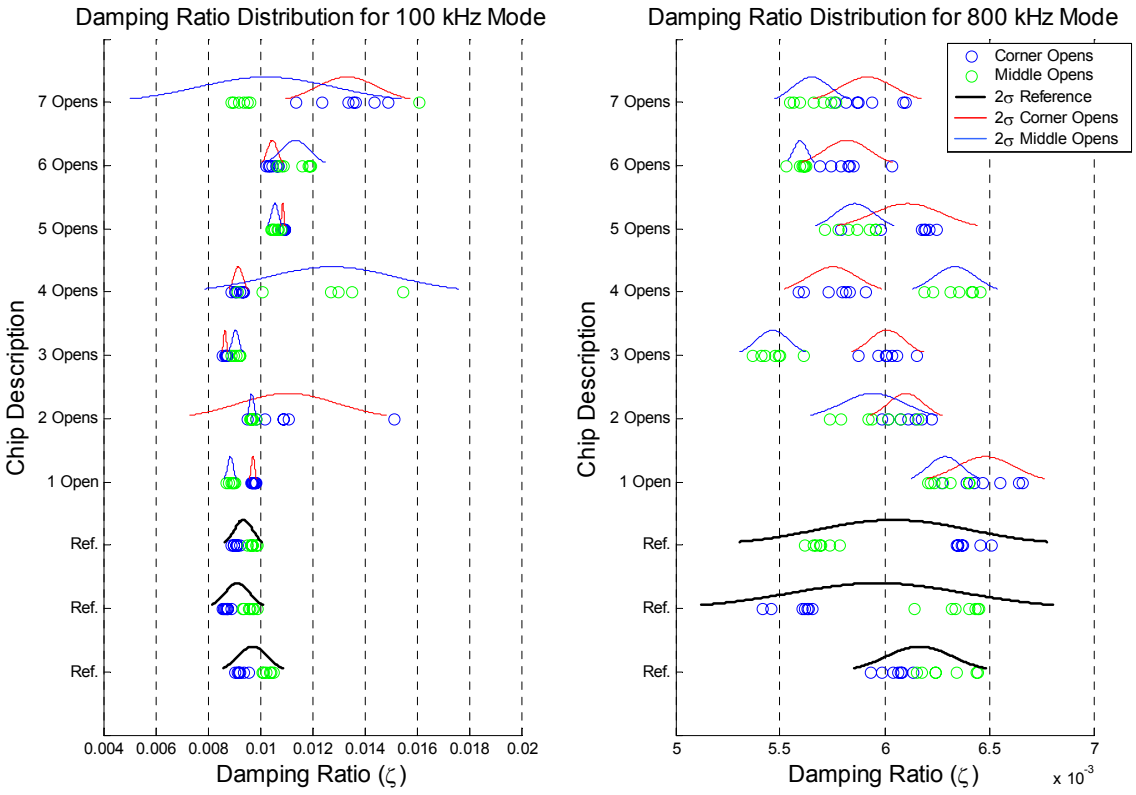


Figure 7-3: Damping Ratio Distribution for 100 kHz and 800 kHz Modes on Both Board Designs

Although the natural frequency and damping ratio for these two modes do not indicate the presence of open solder bumps, the mode shape for each of these modes can be plotted as a function of position on the surface, referenced to the location of the sequential inspection points. Figure 7-4 shows the normalized 100 kHz mode shape for each of the chips with open solder bumps starting from the corner on Board Design 1, having open solder bumps starting from a corner. Each defective chip is represented with a colored line, and mode shapes for the three reference chips were averaged together and plotted with positive and negative 2σ lines to indicate the threshold between reference

chips and chips with open solder bumps. From this plot, a clear change is visible near inspection point number 36, which is the corner nearest the series of intentionally created open solder bumps.

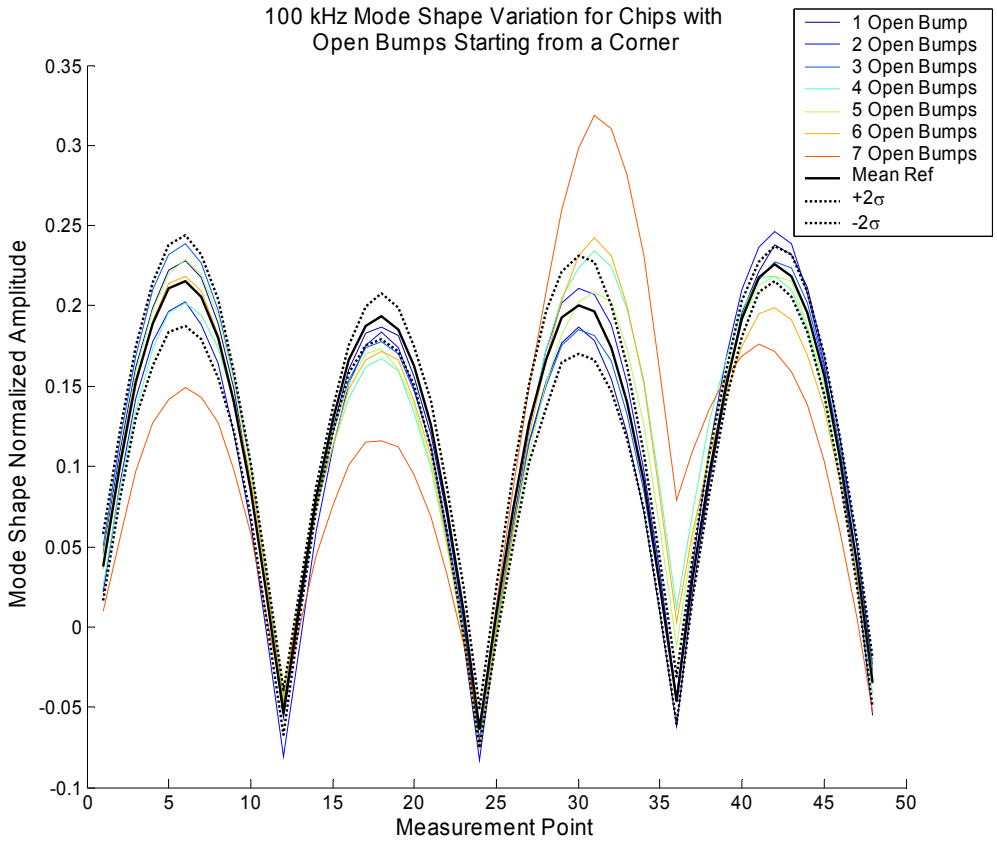


Figure 7-4: 100 kHz Mode Shape Changes for Chips on Board Design 1 (Open Bumps Starting in Corner).

Figure 7-5 shows a zoomed in view of the corner closest to the start of the sequence of open solder bumps on Board Design 1. Although the mode shapes are very consistent at points far removed from the location of the defects, the decrease in

boundary condition stiffness at the location of the defects causes an increase in the displacement of the chip's surface. Based on the data shown here, a chip with three or more adjacent defect will be detectable using the mode shape information calculated along the location of the inspection points.

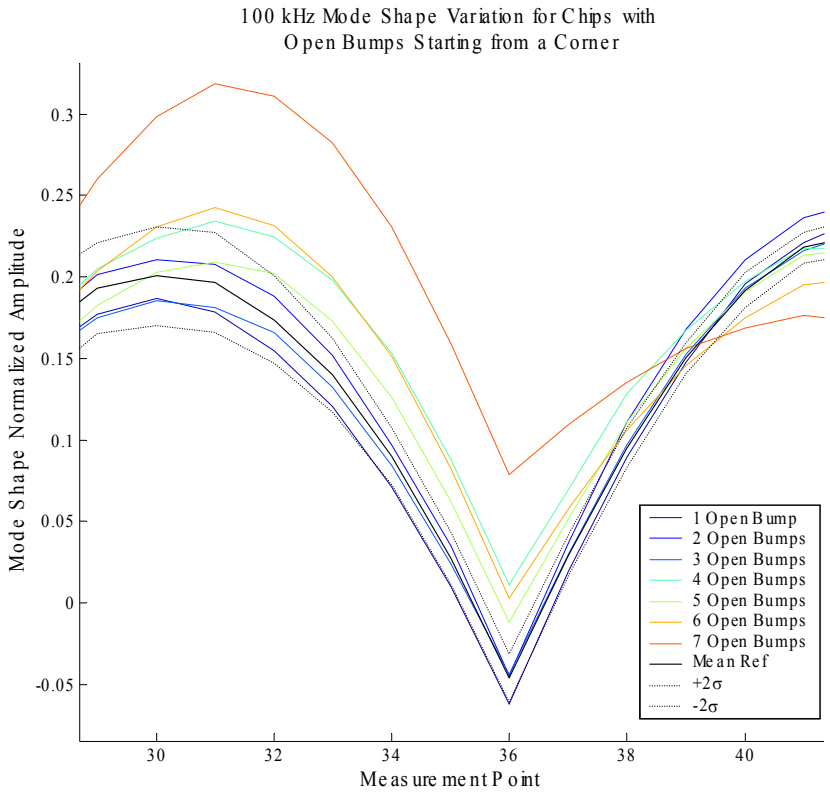


Figure 7-5: Detail View of Average Reference 100 kHz Mode Shape Compared with All Chips on Board Design 1 Having Intentionally Created Open Bumps Starting from the Corner of a Side.

The mode shapes for the chips attached to Board Design 2, having open solder bumps starting from the middle of the side, are shown in Figure 7-6 and Figure 7-7.

Because the open solder bumps start from the middle of the side, the mode shapes are different than were observed for the chips on Board Design 1. The highest amplitude and the greatest difference between the average reference mode shapes and the chips with open solder bumps occur in the middle of the side, near inspection point 30. The effect of the open solder bumps is localized to the side on which the bumps are open, requiring that for detection the number of inspection points will have to be at least 48. Having fewer inspection points will increase the chances of missing a defect.

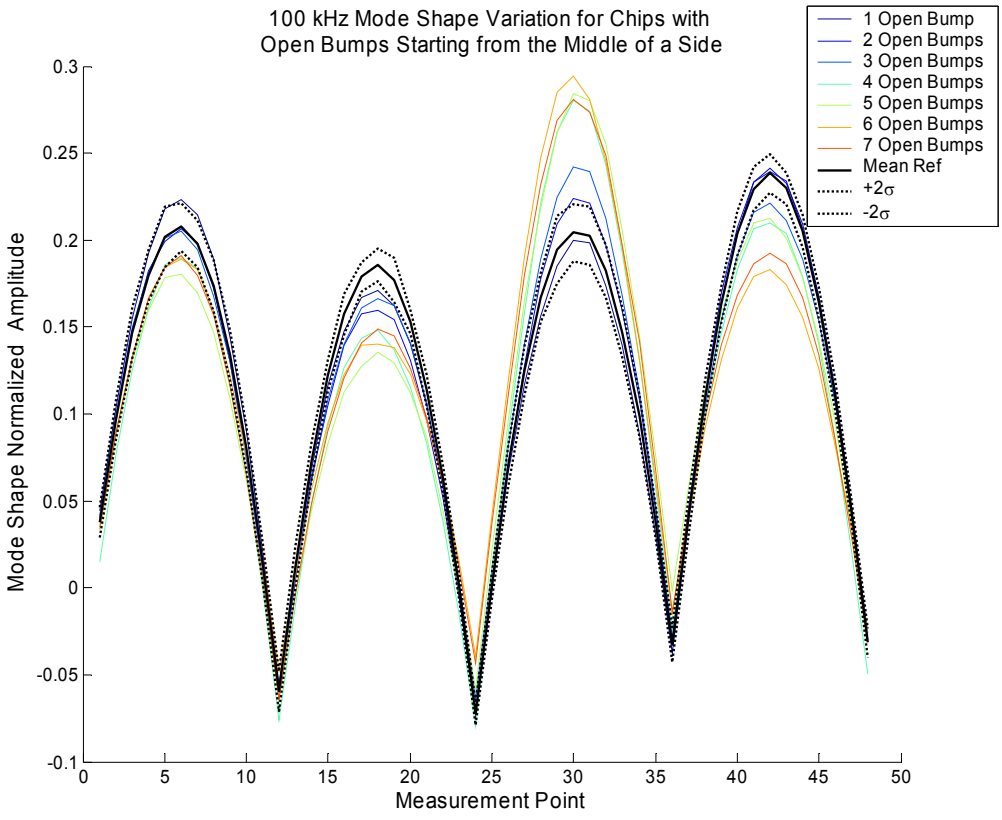


Figure 7-6: 100 kHz Mode Shape Changes for Chips on Board Design 2 (Open Bumps Starting in Middle of a Side).

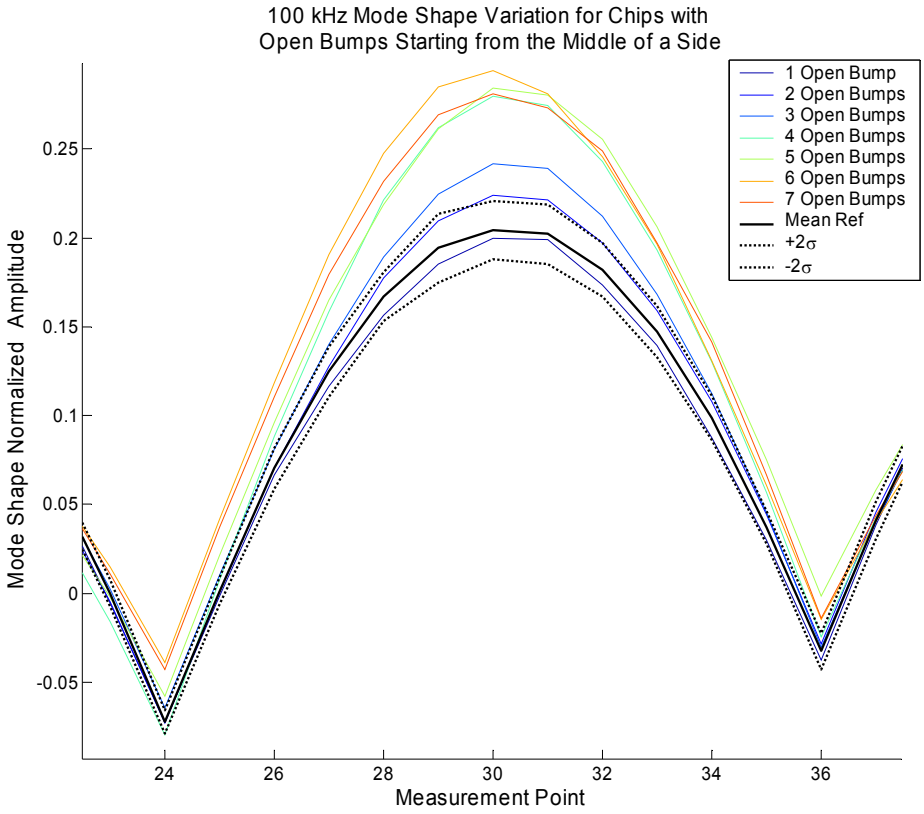


Figure 7-7: Detail View of Average Reference 100 kHz Mode Shape Compared with All Chips on Board Design 2 Having Intentionally Created Open Bumps in the Middle of a Side.

A common technique used to compare mode shapes to ensure you are looking at the same mode is called the modal assurance criterion (MAC) (Allemang, 2002). The MAC value is a measure of how similar two mode shapes are to each other. Therefore, one mode shape has to be selected as a reference, and the rest of them can be compared with that mode shape. For the data shown in Figure 7-8, the 100 kHz mode shape from the reference chips was averaged together to form the reference mode shape vector. For each flip chip on both of the boards, the 100 kHz mode shapes from seven trials were

averaged, and the values for each of the chips are presented. The value for the reference chips is lower than the MAC values for most of the chips with open solder bumps. With increasing numbers of adjacent open solder bumps, the changes in mode shape are similar to the changes observed from the mode shape plot in Figures 7-4 through 7-7. Three or more adjacent open solder bumps can be identified, but chips with one or two open solder bumps have a MAC value that is similar to the MAC values from the reference chips. Therefore, they may not always be correctly identified.

The mode shapes for the 800 kHz mode are presented in Figures 7-9a and 7-10a. The detailed view of the region near the open solder bump locations is presented in Figures 7-9b and 7-10b. The average of all the reference mode shapes are shown with 2σ limits, in the same manner as the mode shapes for the 100 kHz mode shown in Figures 7-5 and 7-7. For the chips with open solder bumps starting from the corner of a chip and the chips with open solder bumps starting from the middle of a side, all of the mode shapes presented by these plots fall within the 2σ limits on the average mode shapes from the reference chips. Although the 800 kHz mode is very consistent from chip to chip and board to board, it cannot be used as a discriminating factor for the detection of open solder bumps because the mode shape does not change in response to open solder bumps. Because the mode shapes for this mode were so consistent, the MAC values for the data were not computed. The similarity between the data prevents the MAC values from being useful.

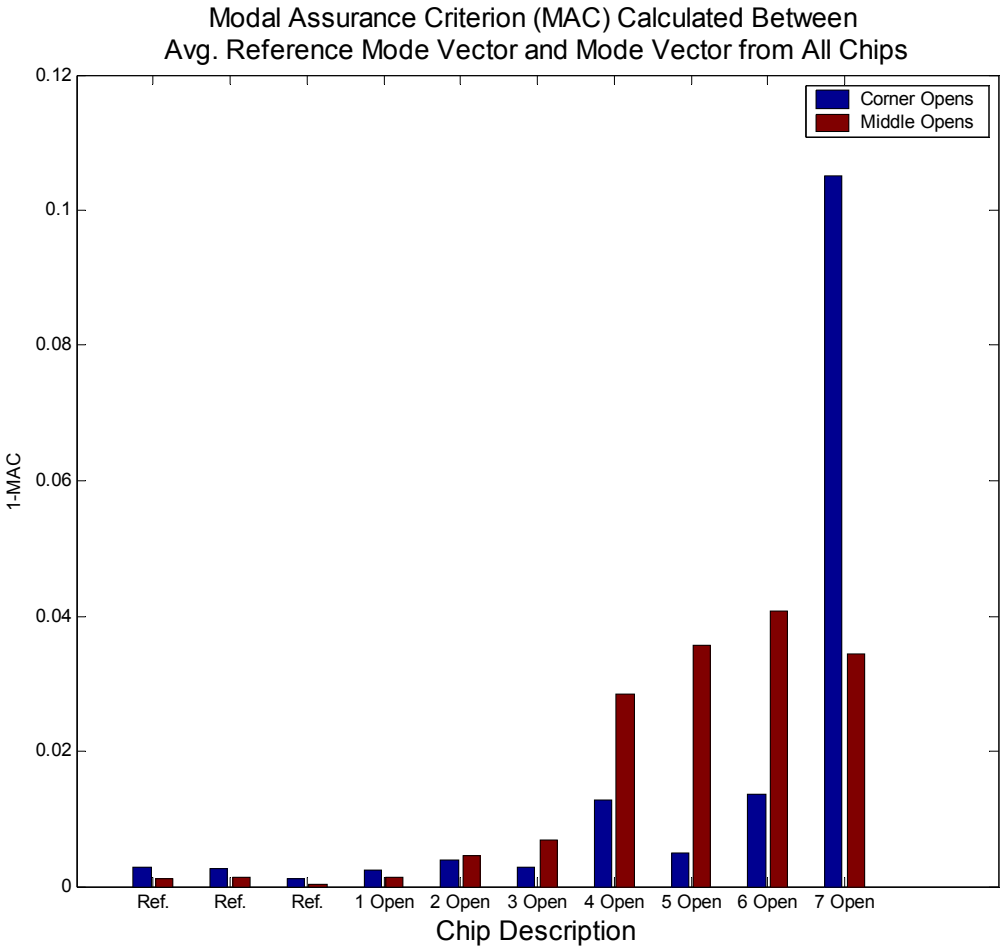
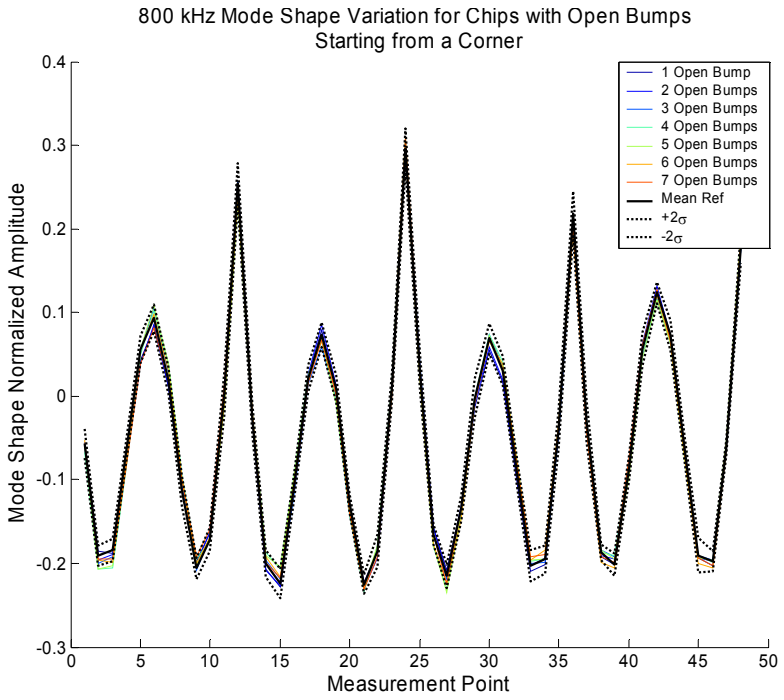


Figure 7-8: Modal Assurance Criterion (MAC) Values for Every Chip in Comparison to the Average Reference Chip (Chips 4, 5, and 8 have no open bumps) with the 100 kHz Mode.



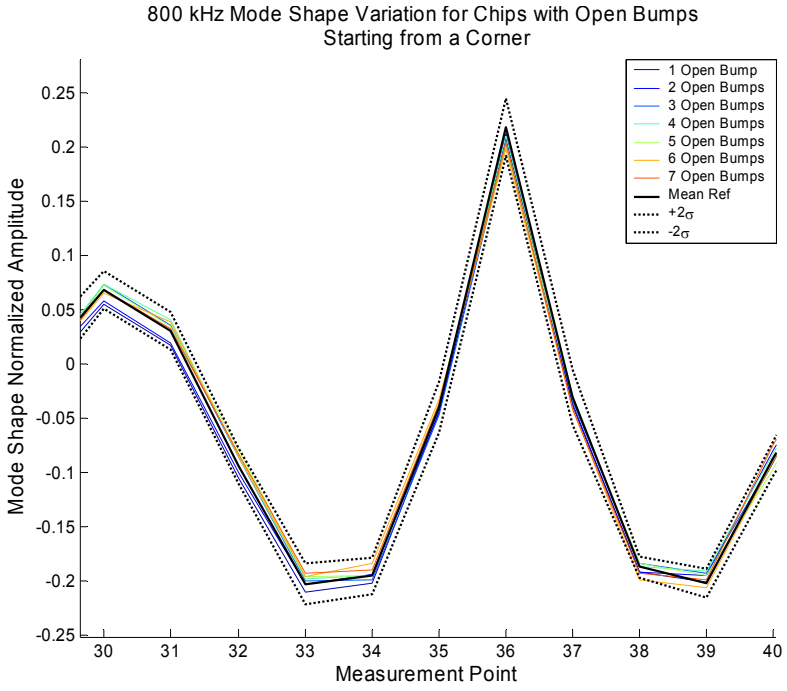


Figure 7-9: 800 kHz Mode Shape for Chips with Open Bumps Starting from a Corner a.) Full View and b.)Detail View of Location of Open Bumps

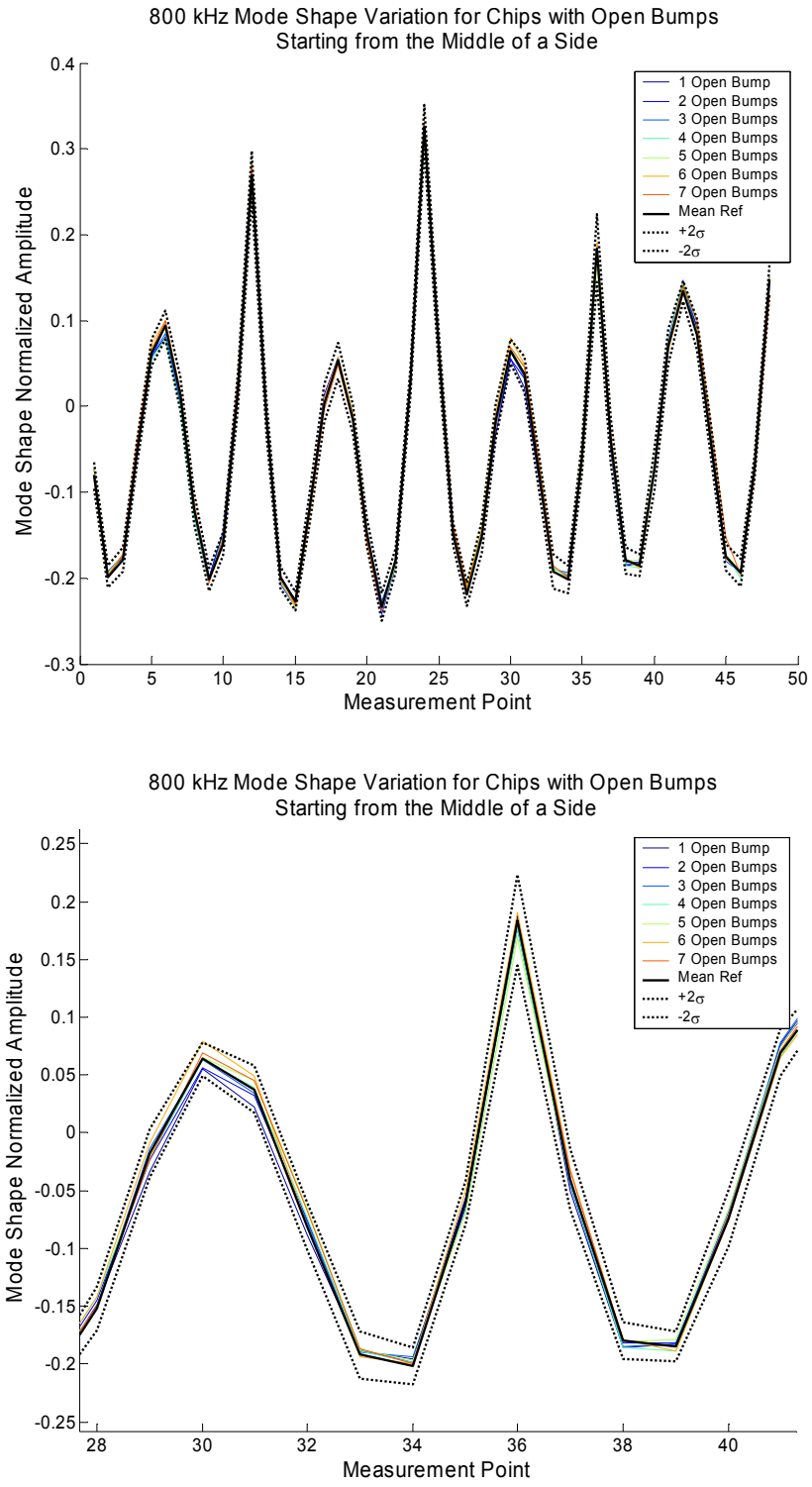


Figure 7-10: 800 kHz Mode Shape for Chips with Open Bumps Starting from the Middle of a Side a.) Full View and b.)Detail View of Location of Open Bumps

The structural modal analysis approach using the AMI method has proven to be useful in identifying the presence of open solder bumps between a flip chip and the circuit board. However, the most basic approach of monitoring the natural frequency values and damping ratio values is not definitive in determining the difference between reference chips and defective chips because the manufacturing variation between chips is too great. Although several modes can be extracted, the 100 kHz mode and the 800 kHz mode were the most consistent. Unfortunately, the 800 kHz mode is too stable, as it did not change in response to any defects. The 100kHz mode shape on the surface has been shown to be effective in discriminating between reference and defective chips, and the MAC also provides a convenient method of looking for changes to the mode shape.

CHAPTER VIII

FINITE ELEMENT MODEL OF FLIP CHIP VIBRATION RESPONSE

To supplement the experimental understanding of the modal behavior of the flip chip package, a finite element model was created to simulate the same defects that were tested in the original package. There are two goals in the implementation of the modal model: to verify the modes detected in the experimental phase of the research, and to identify other modes that were not detected that may help increase defect resolution. A solid model was created of the chip, modal analysis was performed, and model parameters were optimized for more accurate results. The results from the modal model match the experimental values closely, and they identify several other vibration modes that are not being excited using current methods.

8.1 Justification

Although several types of models can be generated to perform modal analysis, the finite element method was chosen for this application. Analytical models for vibration analysis have been used for plates undergoing bending (Gorman, 1982), however, an analytical model that captures the vibration modes for a continuous plate is not a trivial problem. Therefore, the decision was made to pursue a finite element model of the

system, to avoid some of the complications with an analytical model. For the current research, this choice is not unprecedented, as it follows the work done by Liu, 2000.

8.2 Model Creation

A complete solid model of the flip chip with 48 solder bumps was created and meshed. Typical symmetry conditions were not applied in this situation because the entire system becomes asymmetrical when one solder bump is left open (unconstrained). However, a symmetric model could be used for the reference chips. The goal is to compare the model results with the different types of defective chips, so the full model is used for every condition being considered.

In order to create a model of the system that captures vibration response changes, the important features are different than are necessary for a more traditional models. Simplifying assumptions are made to allow for creation of the model within the limitations of the software package and the ability of the properties to be verified. The assumptions are listed below.

8.2.1 Assumptions

1. Silicon die is a homogeneous piece of silicon material.
2. The under bump metallurgy (UBM) material is inconsequential to the model, and the solder bump is directly attached to the chip.
3. The natural vibration frequencies of the chip are sufficiently higher than the vibration frequencies of the board to prevent coupling. Therefore, the model

neglects the FR-4 board and assumes that the bottom of the solder bumps are fixed in the X, Y, and Z directions.

4. To account for small material and geometry variations, an optimization of several parameters was performed to adapt the model to the experimental results. These parameters were Si density, chip thickness, and Si Young's Modulus.

5. Minor changes in the size and material properties for the solder bumps did not have a major effect on the overall vibration characteristics.

These assumptions are valid for the model under consideration because the goal is not to exactly determine the thermal, fatigue, or electrical properties. The only goal is to determine the dynamic properties, and to represent the overall characteristics of the device. These simplifications to the model allow for fine meshing parameters and a reasonable solution time. Without the simplifications allowed by these assumptions, the number of elements would exceed the maximum limit allowed by the software package.

The model was created using parameters from the manufacturer and from literature. These properties cover a range of values, but a summary of the geometric and material parameters used in the model is presented in Table 8-1. The thickness of the Si die is thinner than the original wafer, but the value was set from optimization of the modal vibration response in comparison with experimental data.

Table 8-1: Material Properties and Geometry Parameters for Model

Silicon

Property	Value	Units
Density (ρ)	2630	kg/m^3
Modulus of Elasticity (E)	130	GPa
Poisson's Ratio (ν)	0.31	

Solder (Eutectic 63-37 Pb-SN)

Property	Value	Units
Density (ρ)	8340	kg/m^3
Modulus of Elasticity (E)	31.5	GPa
Poisson's Ratio (ν)	0.37	

8.3 Element Selection

Selection of the most appropriate elements is a critical decision in the creation of a finite element model. The elements need to have all the desired parameters required for the solution, the ability to adapt to the geometry of the problem, and elements from different parts of a structure must match at the interfaces between materials.

The most desired element for this model is a SOLID 45 linear, brick element, as shown in Figure 8-1. The brick elements are better at modeling bending, and linear shape functions require fewer node points, reducing the solution time. These elements allow a large change in element size, and they provide control over the size and spacing of the mesh. This element meets the needs of the geometry and modal analysis solver. However, the degenerative forms, which are used when matching meshes between parts of a model, are not capable of providing an accurate transition between tetrahedral and brick elements. This model needed this capability for matching the mapped mesh

portions of the model to the free-mesh portions of the model. Therefore, this element cannot be used for this model.

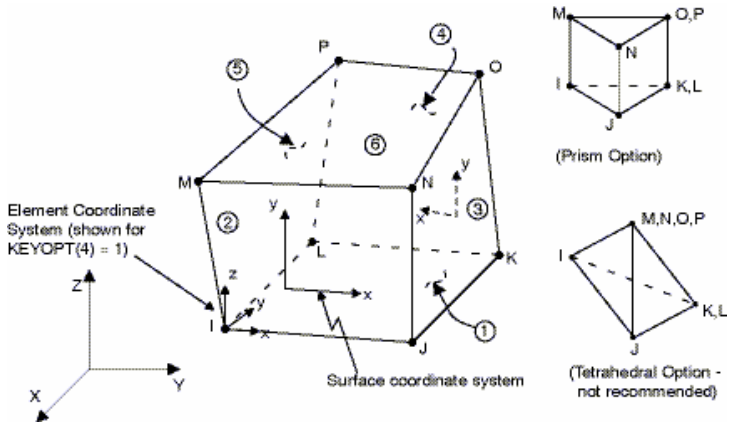


Figure 8-1: SOLID 45 Element Description from ANSYS Documentation

Because of the limitation of the SOLID 45 elements, a more complex element is used to create the mesh for this model. The SOLID95 element, shown in Figure 8-2, is a 20-node, quadratic, brick element. Each edge of the element has three nodes, defining a quadratic equation for the shape of the edge. Because of the twelve additional elements for every element, the final mesh of the model cannot be as fine, and the solution will take longer to run because quadratic equations are more difficult to solve than linear equations. However, one of the degenerative forms of the SOLID95 elements does provide a pyramidal shape that serves as a good interface between brick and tetrahedral elements. Therefore, the selection of SOLID95 elements meets the geometry and solution requirements.

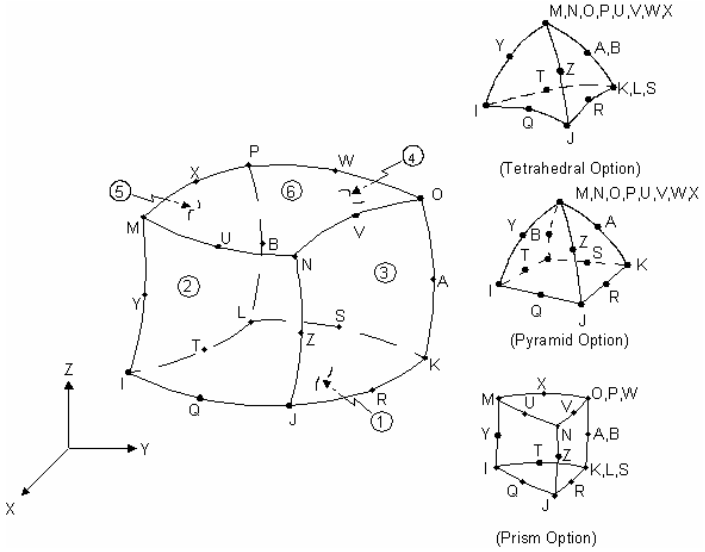


Figure 8-2: SOLID 95 Element Description from ANSYS Documentation

8.4 Solder Bumps

The solder bumps are modeled from a 2D cross-section, and then the cross-section is swept into eight separate volumes around the central point. The mesh is created by meshing the top of the bump with two-dimensional, four-sided elements and then sweeping the mesh from the top of the bump to the bottom of the bump, providing a consistent and controlled meshing procedure for each bump. Consistency and control prevent meshing differences from changing the results calculated for individual bumps.

The two-dimensional element used to mesh the top surface of the solder bumps is the PLANE82 element in ANSYS, as shown in Figure 8-3. The element is an 8-node, quadratic, rectangular element, having four sides with quadratic shape functions on the edges. Although the element can degenerate into a triangular option, that option is not

used. The rectangular option is desired for matching the mesh between the solder bumps and the silicon chip.

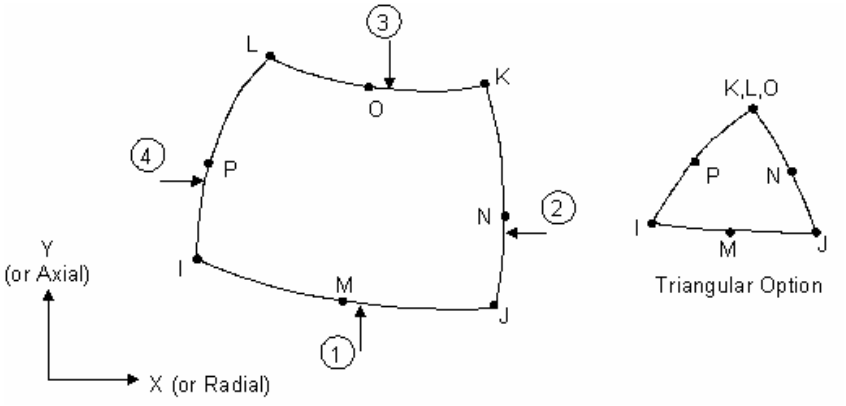


Figure 8-3: PLANE82 ANSYS Element for Creating Mesh to Sweep Through Solder Bumps

Using the PLANE82 elements to create an area mesh at the boundary between the solder bumps and the chip provides control over the number of elements in each bump, as well as preventing meshing errors that occur when a free mesh is applied to such small volumes. In addition, the two-dimensional mesh is automatically transferred to the silicon chip, providing a predictable interface between the bumps and the chip. Figure 8-4a and Figure 8-4b show the unmeshed and meshed solder bumps. The solder bumps were meshed with the SOLID 95, 20-node, quadratic, brick element, as previously described. Each solder bump has approximately 44 elements within the volume, so the shape of the bumps is very close to the original geometry.

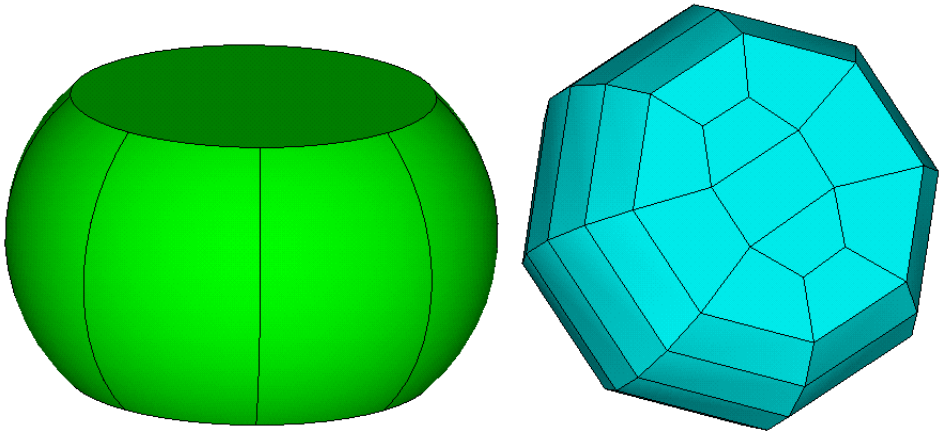


Figure 8-4: Solder Bump Model a) Unmeshed and b) Meshed

Although the PLANE82 elements are useful for controlling mesh generation during the creation of the model, they do not add to the desired solution. Therefore, the PLANE82 elements are deleted after the mesh has been generated on the chip volume, removing them before the solution is calculated.

8.5 Silicon Chip Sub-Modeling

To provide a consistent and controllable mesh, the silicon fb250 test die is modeled and meshed in two separate parts, called sub-models. Figure 8-5 shows a view of the bottom of the silicon chip. The exterior ring, in light blue, has circular attachment points defined for the solder bumps that were created when the solder bump were attached to the chip through a Boolean operation. The circles are sub-areas of the surface of the chip volume that have been defined to remain attached to the solder bump volumes. The interior of the chip, in green, is a solid rectangular block of silicon.

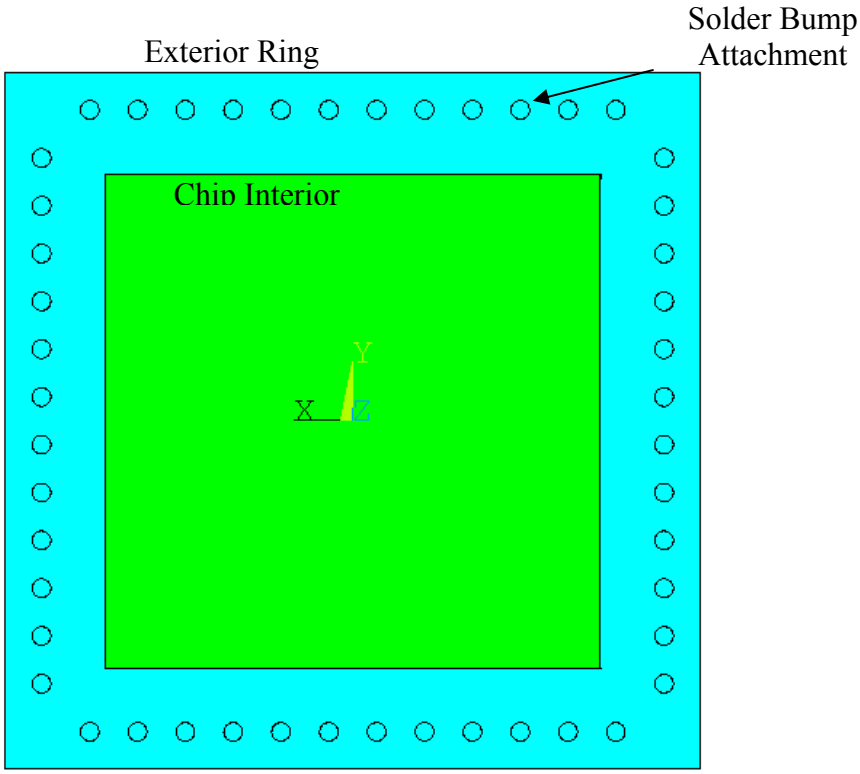


Figure 8-5: Sub-models of the fb250 Test Die

The center of the chip, away from the solder bump attachment points is homogeneous, allowing a mapped mesh to be applied for finer control over mesh generation. A mapped mesh has regular spacing and consistent size and shape for the elements, preventing typical mesh generation errors. The mapped mesh for the central area of the chip is shown in Figure 8-6. This portion of the chip is meshed in two layers with the SOLID 95 linear brick elements. Tetrahedral elements with triangular faces can be too stiff when trying to model flexural displacements, so the linear brick elements provide more accurate results.

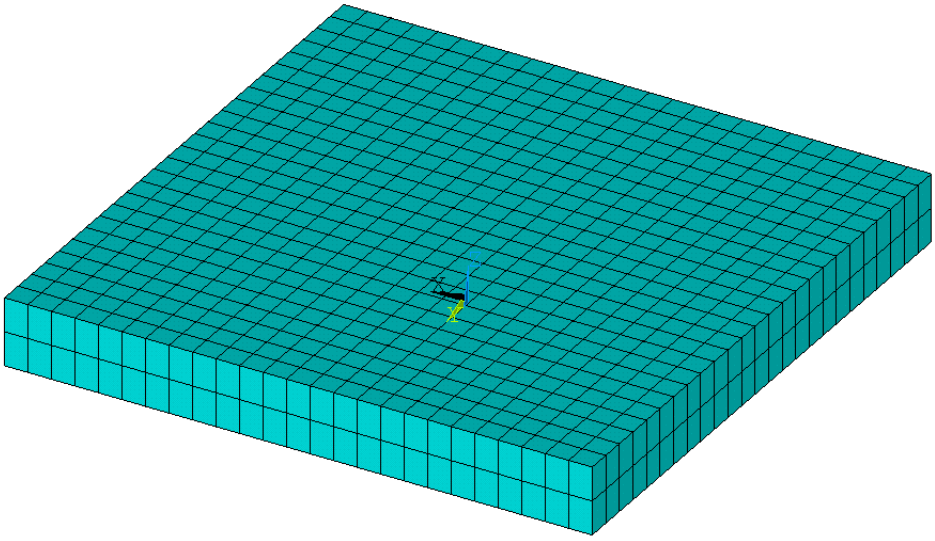


Figure 8-6: Mapped Mesh of Chip Interior Sub-Model

The outer ring attaches to the solder bumps, so the geometry includes areas that are defined on the bottom surface for attachment. Definition of these small areas on the surface of the volume prevents mapped mesh generation because the automated meshing tools in ANSYS do not know how to handle the sub-areas on the bottom of the chip that are attached to the solder bumps. Therefore, a free mesh is applied to this volume, giving automated control of the meshing to ANSYS and requiring the use of tetrahedral elements to handle the complex geometry. The transition between the small elements in the solder bumps and the large volume of the chip requires a large number of small elements that grow in size to match the mesh of the chip's interior. The meshed outer ring is shown in Figure 8-7a and 8-7b, and the transition from small to large elements between the solder bump attachment points and the edges of the model are evident.

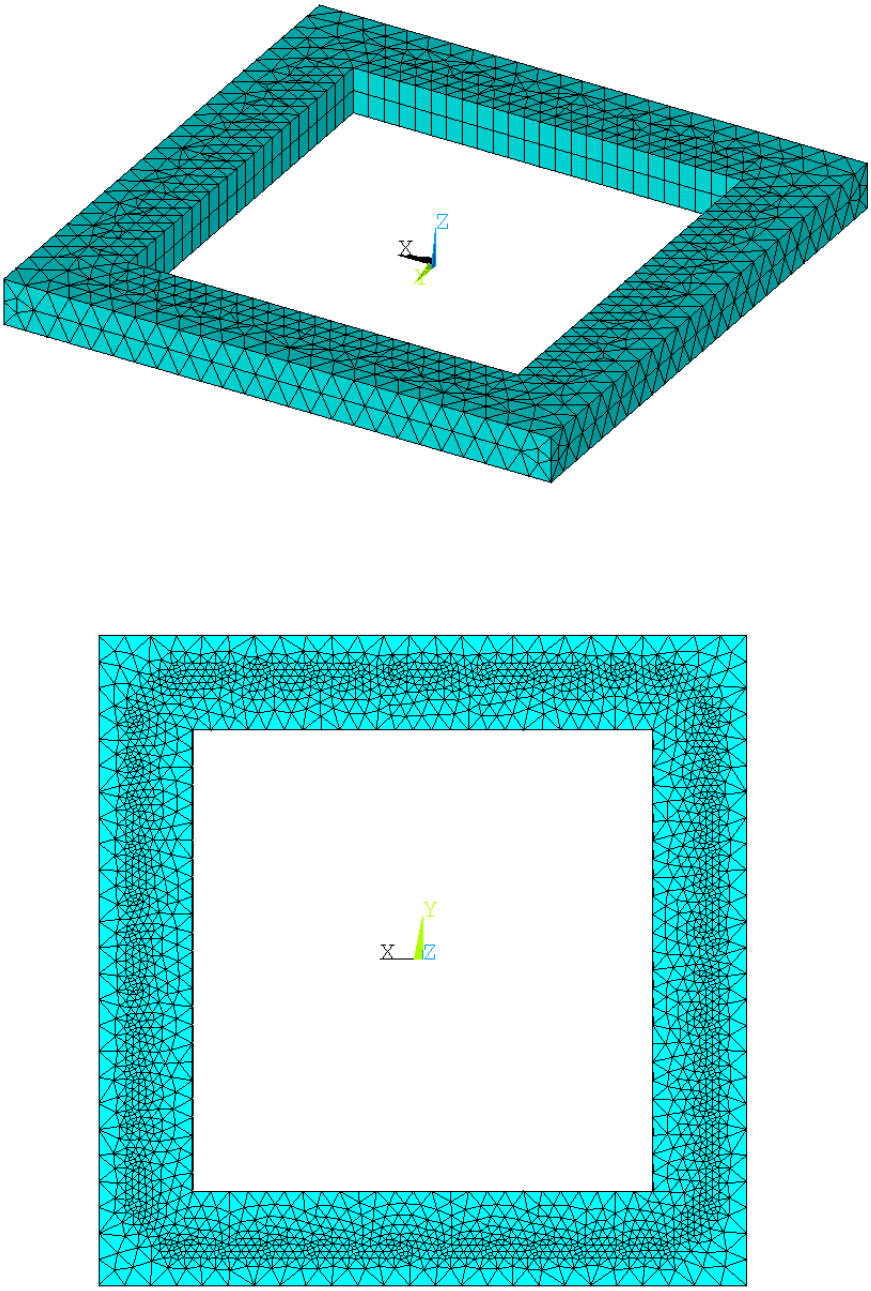


Figure 8-7: Free Mesh of fb250 Test Chip Outer Ring with a) Isometric View and b) Bottom View

The volume is meshed with SOLID 95 linear tetrahedral elements. However to match the mapped mesh on the chip interior volume, which have four-sided faces, the

alternative form of a pyramidal shape is allowed on the boundaries connecting the two chip volumes. The pyramidal form of the SOLID95 elements is shown in Figure 8-2. These transition elements provide the connection between a four-sided linear element and a three-sided element face.

The complete model for the chip with all 48 solder bumps requires 25,000 to over 36,000 elements, depending on the settings for mesh generation. With twenty elements for each element, the maximum number of nodes for the current version of ANSYS is not difficult to exceed. Although some elements share nodes, the maximum number of nodes for the available version of ANSYS is approximately 120,000, restricting the level of detail that can be expected from this model.

8.6 Solution

The finite element portion of this research is based off of a modal analysis package inherent to the ANSYS software. This package finds the natural vibration modes for an object based on geometry, mass distribution and material properties that provide parameters for the stiffness matrix for the structure.

The solution process is automated, and the first 60 modes are extracted through the Block Lanczos modal analysis solver. The solver provides a mathematical solution, calculating modes in all six degrees of freedom. However, the laser interferometer measurement only allows detection of modes that have strong vibration response in the direction normal to the chip surface. Therefore, out of the 60 modes, which are extracted from the analysis, only a few of them can be compared with the experimental results.

8.7 Optimization

In order to get the most accurate modal analysis solution, the geometric and material properties must be accurate. Unfortunately, there is not a completely predictable response for changes in these values, so an automated optimization routine was created to find the best set of values. This routine looks at the modal vibration frequencies extracted from a modal analysis and compares them with experimental data presented in Table 8-2.

Table 8-2: Modal Frequency Set Points for Finite Element Optimization

Model Mode	Frequency Setpoint (kHz)
1	101.690
3	199.945
7	252.100
24	798.340
48	1081.350

Each of these modes was compared with the set point from the data extraction, and the values were normalized to be a percentage away from the desired value. Converting the error in the modes to a percentage gives each of the modes an equal weight in the final optimization function. The percentage of error from each of the five modes was added together to create a total optimization value. The ANSYS optimization functions iteratively solve to reduce the optimization score by changing the design variables.

For this analysis, the design variables were selected based on the sensitivity of the model to changes in the design variable and the uncertainties in the parameters used to create the model. To avoid excessively long computing time, the design variables are limited to three values: density of silicon, thickness of the silicon chip and the Young's Modulus of silicon. Changing these values slightly causes a significant change in the vibration frequency and the mode shapes. Despite limiting the optimization to only three variables, the total solution time was more than 30 hours of computing time.

Once the optimization solution converged, final values were selected for the three design variables. For the rest of the trial cases of the finite element model, all of the model parameters are fixed. Only boundary conditions on the elements are changed, in order to simulate the presence of open solder bumps. The final values for the three design variables are shown in Table 8-3. These values fall into the preset ranges for the design variables, so an acceptable solution was found within the design space.

Table 8-3: Finite Element Model Optimization Results

Silicon

Property	Starting Value	Ending Value	Units
Density (ρ)	2630	2638	kg/m^3
Modulus of Elasticity (E)	130	120.3	GPa
Poisson's Ratio (ν)	0.31	0.31	
Chip Thickness	635	562.6	(μm)

The values for the dimensions and properties of the chips did not not change very much, however, the mode shape did change appreciably from the reference (fully constrained) condition to the model with seven adjacent bumps left unconstrained. Displacement data was obtained along a path around the top surface of the chip, as shown in Figure 8-8. This path contains all of the inspection points from the experimental data, so the results can be directly compared.

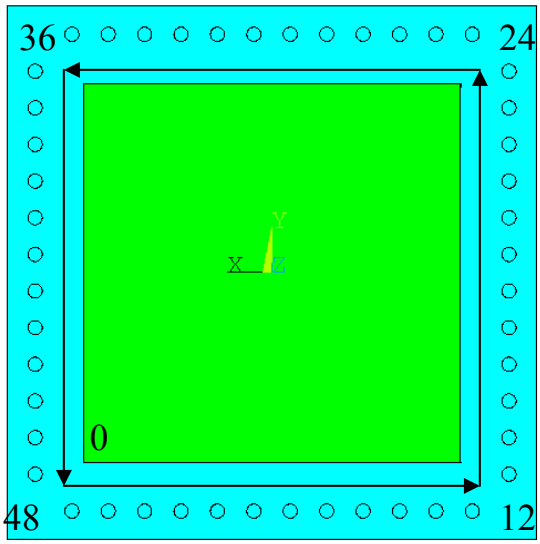


Figure 8-8: Surface Displacement Output Path

Although displacement data is available along the pre-defined path, the first comparison with experimental data must be made with the natural frequency values, which are listed in Table 8-4. These values show a trend in the natural vibration frequency with an increasing number of defects, and this matches a similar trend observed from the experimental data. However, changes on the order of 100 Hz cannot

be effectively measured. Therefore, this is not the best method to use for comparing the results between the model and the experimental data.

Table 8-4: Modal Analysis Frequency Results

Model	Mode 1 (kHz)	Mode 3 (kHz)	Mode 7 (kHz)
Reference	**103.375**	**164.987**	**328.291**
1 Open Corner	103.227	163.503	327.501
2 Open Corner	103.109	161.802	319.863
3 Open Corner	102.864	159.822	290.044
4 Open Corner	102.274	157.725	264.254
5 Open Corner	101.014	155.577	254.383
6 Open Corner	98.618	153.138	251.523
7 Open Corner	94.626	149.693	250.716
1 Open Middle	102.775	163.259	328.052
2 Open Middle	101.931	161.318	327.885
3 Open Middle	100.803	159.149	325.109
4 Open Middle	99.131	156.95	315.48
5 Open Middle	96.946	154.469	293.408
6 Open Middle	93.767	151.759	282.487
7 Open Middle	89.89	148.124	274.237

For the finite element analysis, the frequency change caused by open solder bumps is observable. However, the resolution of the experimental modal extraction is about 1.2 kHz under optimum conditions, based on a sampling rate of 25 MHz of the vibration signal. The frequency resolution decreases further because of uncertainty in the calculation of the natural frequency from the data and from different samples. Although the small change was not observable from the experimental data, the gradual decrease in

frequency for each mode follows the experimental observation. The model output is in agreement with the experimental values. The changes in the vibration frequency are difficult to observe, and therefore, they are not a good indicator of the presence of open solder bumps.

Experimental data analysis using the modal extraction technique showed that the mode shape was more sensitive to the presence of open solder joints. Therefore, the modal displacement of the model was produced for comparison. The finite element model has more complete mode shape information than the experimental data, so the entire chip is plotted at one time, as shown in Figures 8-9 through 8-11 which show modes 1, 3, and 7 for the reference chip.

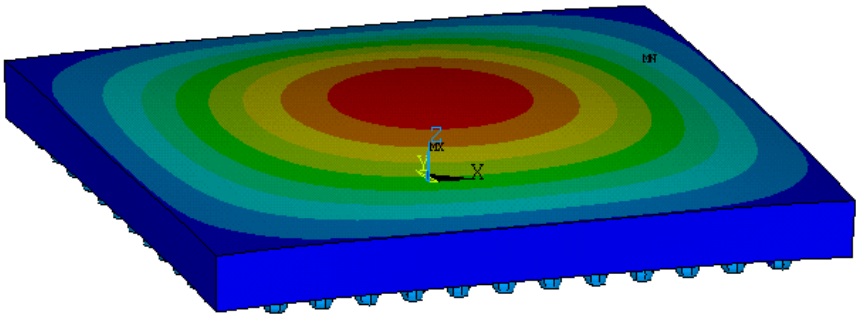


Figure 8-9: fb250 Reference Chip (Mode 1)

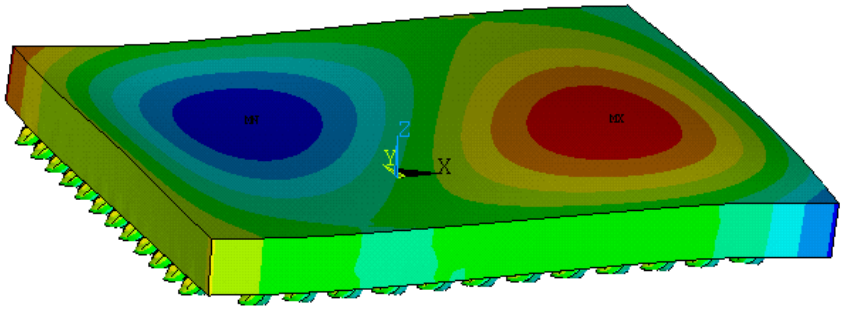


Figure 8-10: fb250 Reference Chip (Mode 3)

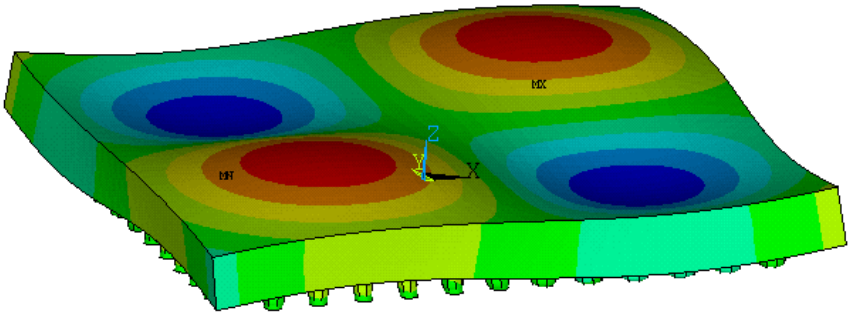


Figure 8-11: fb250 Reference Chip (Mode 7)

The modes are significantly different from each other, and they all have a large component of vibration displacement in the direction normal to the chip's surface. Therefore, these are modes that can be observed with an interferometer directed at the top surface of the chip. Although these modes are different, the changes in the mode shape are harder to observe, when comparing these shapes to mode shapes calculated from a model with 7 open solder bumps in the middle of a side, as shown in Figures 8-12 through 8-14.

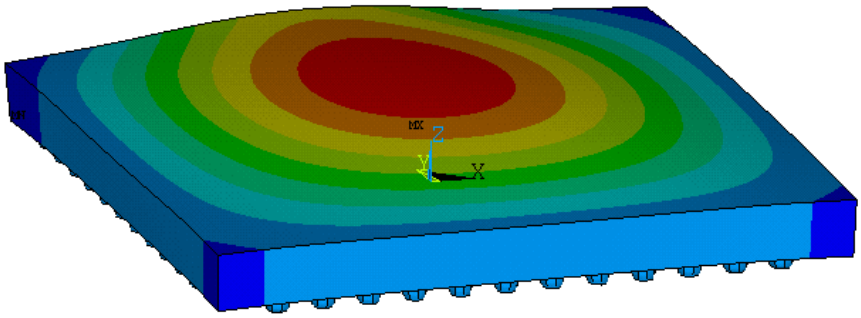


Figure 8-12: fb250 Model with 7 Opens in the Middle of a Side (Mode 1)

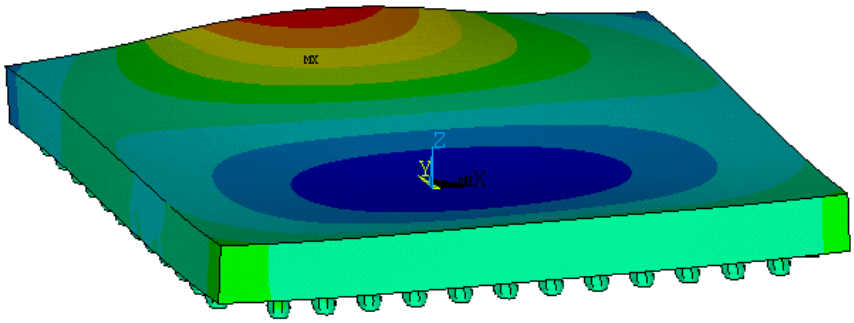


Figure 8-13: fb250 Model with 7 Opens in the Middle of a Side (Mode 3)

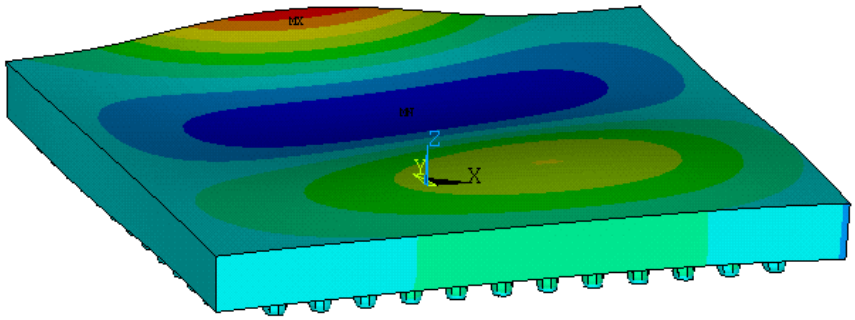


Figure 8-14: fb250 Model with 7 Opens in the Middle of a Side (Mode 7)

Modes 3 and 7 have changed so much that they are practically unrecognizable; however, mode 1 has the same general shape with an accentuated displacement in the middle of the side with seven unconstrained solder bumps.

Because direct comparison of mode shape information shown in Figures 8-9 through 8-14 is hard to achieve, the maximum displacement along the path on the surface of the chip, defined in Figure 8-8, will allow a more direct comparison of the change in mode shape. The path coincides with the inspection points used in the experimental investigation, so the model output will match the experimental results as much as possible. Figures 8-15 and 8-16 show the change in mode shape along the path, as the number of adjacent unconstrained solder bumps is changed from one to seven. This change provides a more distinct means of observing the change in vibration behavior for the model, and it compares well with the trends seen from the experimental analysis.

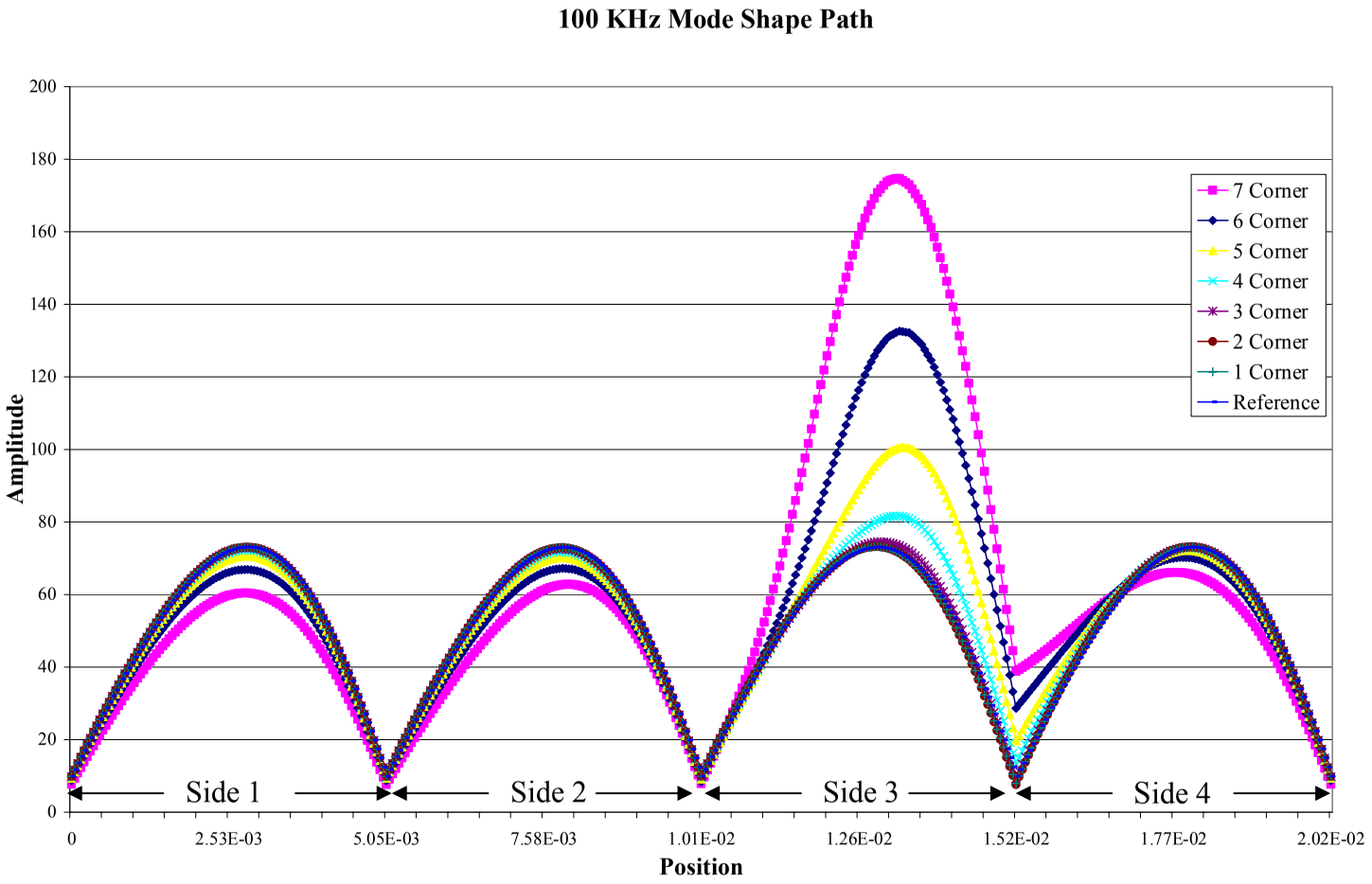


Figure 8-15: FEA Mode Shape Changes Along Path on Surface of Chip for Models with Open Bumps in the Corner

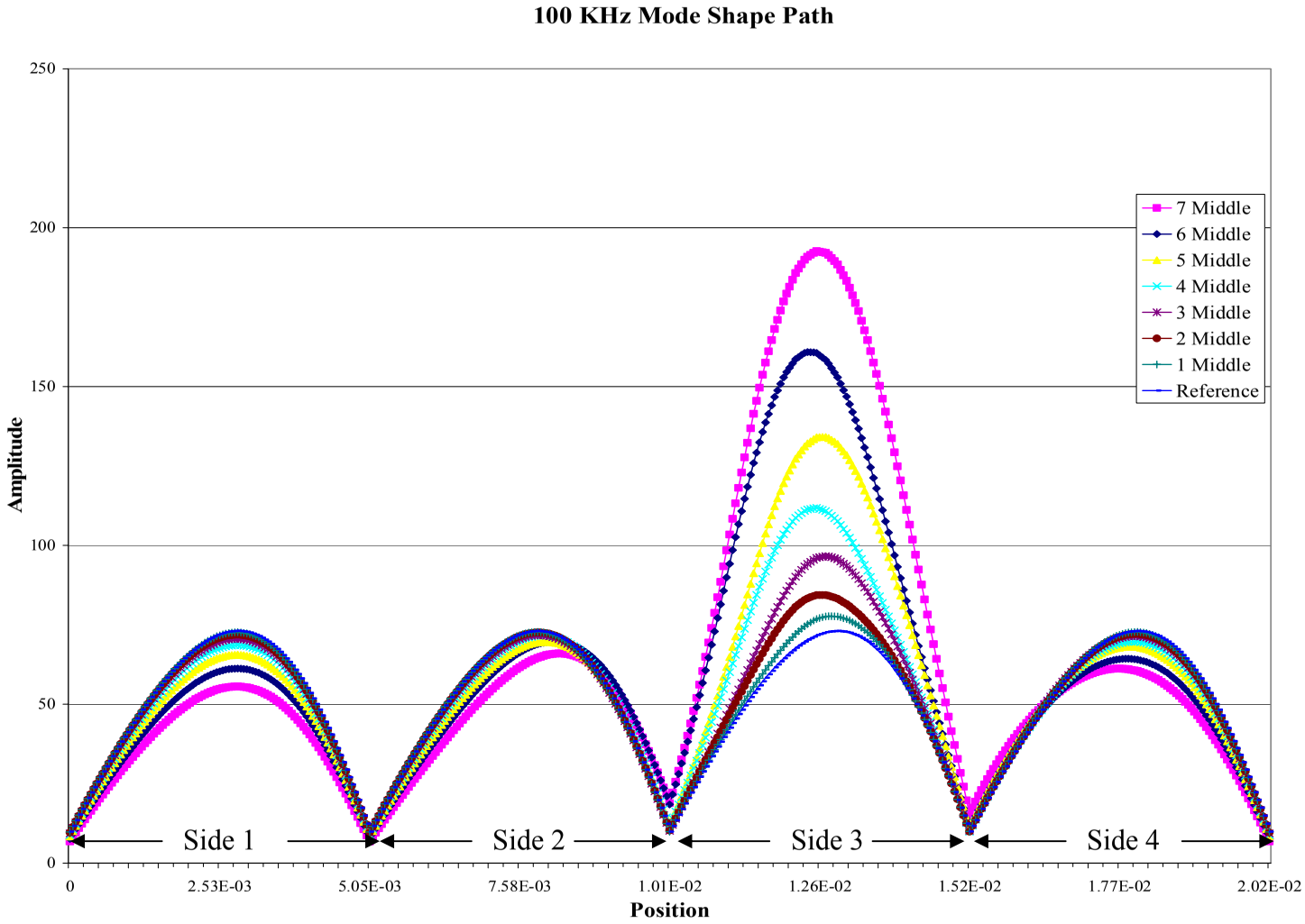


Figure 8-16: FEA Mode Shape Changes Along Path on Surface of Chip for Models with Open Bumps in the Middle of a Side.

Although the trend shown in Figures 8-15 and 8-16 follows the logical assumption of more displacement with fewer constraints, the data does not compare precisely with the data extracted from the experimental specimen responses. The uncertainty with the experimental responses prevents the small change in displacement from being observed, however, the trend is consistent and can be used as an indicator of the presence of open solder bumps.

From the finite element analysis results and the experimental analysis, the frequency and damping ratio have been shown to be poor indicators of the presence of open solder bumps in the flip chip package. Frequency resolution is currently too low and the data is too scattered to use the natural vibration frequency shift as a positive indicator of the presence of defects. The natural frequency is too susceptible to changes in the part geometry, excitation, or fixturing. Damping ratio values are even more inconsistent, as the damping ratio is extremely sensitive to small changes in boundary conditions. However, the observed manufacturing variation caused the damping ratio values to be inconsistent between reference specimens. In the finite element analysis, the damping ratio was left out of the model. Therefore, the mode shape along the path defined by the inspection points on the top surface of the chip provides a clear method to determine the presence of open solder bumps.

A complete solid model of the PB-18 fb250 flip chip was created and modeled in ANSYS. This model was used to investigate the modal vibration properties of the package when various open solder bump configurations were introduced. An optimization method was used to ensure that the model was most closely matched to the

experimental results, and the resulting frequencies and mode shapes show similar responses. Therefore, the modal analysis model shows that the damage caused by open solder bumps can be measured using modal analysis techniques by monitoring the change in the mode shape of the chip.

CHAPTER IX

MULTI-LAYER CERAMIC CAPACITOR TESTING AND RESULTS

Three series of experiments were performed on three sets of MLCC samples. For each set of samples that were mounted on flex-testing boards, some samples were provided as-manufactured, and other samples were flex-tested to failure. Initially, a rectangular cross-section 0805 MLCC sample (0.080"x0.050" cross-section) was inspected, using a single excitation spot and a single vibration measurement spot (Erdahl and Ume, 2004). Passband isolation was used to increase the resolution and sensitivity of the Error Ratio values. The flex tested to failure samples were successfully classified as different from the as-manufactured samples. The inspection procedure was repeated for two more sets of MLCC samples that both have square cross-sections, increasing the stiffness and reducing the sensitivity of the inspection procedure (Erdahl and Ume, 2005). Although classification of the flex-tested to failure samples was more difficult, comparison with multiple reference capacitors provided a cleaner separation between the good and cracked samples. This chapter presents a description of the three sets of samples, as well as the data analysis performed to prove the capability of the inspection method to detect these defects.

9.1 MLCC Test Vehicles

The test vehicles are described in two batches, as the parts were assembled in two different manufacturing runs. The first set of samples, rectangular cross-section 0805 MLCCs, was assembled as a single batch (Erdahl and Ume, 2004). The second set of samples, square cross-section 0805 and 0603 MLCCs, were assembled at the same time (Erdahl and Ume, 2005). Portions of all three sample sets were flex-tested to failure prior to delivery for laser vibration testing.

9.1.1 0805 Rectangular Cross-Section MLCCs

The first batch of samples was provided to test the capability of the system to detect flex cracks in MLCCs. Samples of a specific 0805, 100 nf, 50 V, X7R capacitor, having a rectangular cross-section, were selected because they are susceptible to flex-cracking. Twenty test capacitors were supplied from the same lot, and they were all mounted on separate organic substrate boards, shown in Figure 9-1, also from a single lot. These boards are special flex testing boards for measuring deflection while monitoring capacitance, so the onset of forces that repeatably cause flex cracks can be found (Bergenthal, 1998). Because designing manufacturing processes to avoid excessive bending stress is the only way to avoid flex cracks, the flex-testing procedure is implemented to measure this susceptibility (Bergenthal and Prymak, 1995). All of the parts were assembled in one batch, and they underwent reflow at the same time in order to minimize manufacturing process variation. After assembly, ten of the sample boards were set aside to maintain an "as-manufactured" condition, and the other ten sample boards were flex-tested until failure was measured as a capacitance drop (Bergenthal and

Prymak, 1995). By selecting the samples from a single lot, process-induced manufacturing variations are minimized, and the flex-testing, performed until failure, ensures that damage caused by flex cracks will dominate the vibration response in the system. The carefully controlled set of MLCC samples provides a means of testing the system and techniques before attempting to identify all of the potential process-induced defects that can be found in a manufacturing facility.

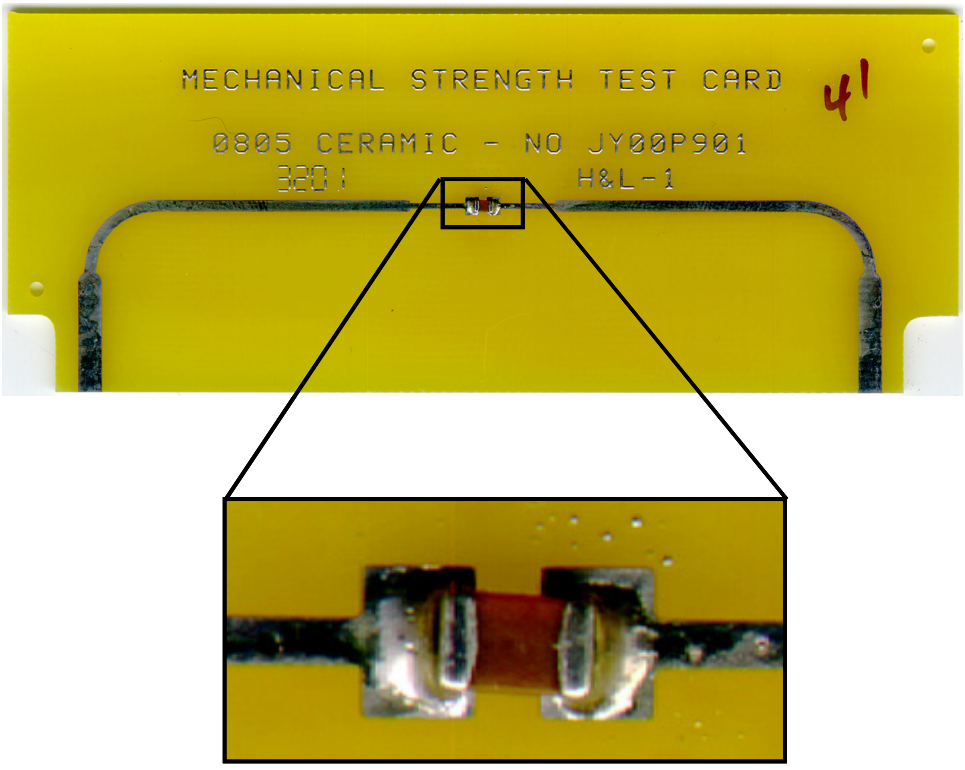


Figure 9-1: Picture of MLCC Flex-Testing Sample (0805)

9.1.2 0805 and 0603 Square Cross-Section MLCCs

Two additional chip capacitor samples were evaluated using the laser vibration technique. These types include an 0805, 10 μF, 6.3 V, X5R capacitor with a square cross-section, and an 0603, 1 μF, 10 V, X5R capacitor also with a square cross-section. Test samples were supplied for both sets of capacitors, and both the capacitors and the boards were randomly selected from a single manufacturing batch for each size to minimize manufacturing process variability. Each capacitor is mounted on a separate organic substrate board (100 x 40 x 1.58 mm), as shown in Figure 9-1. All of the capacitors were assembled in one batch, under the same conditions, and then some of the test capacitors were set aside to maintain an as-manufactured condition. Other sample capacitors underwent flex testing until failure occurred, as measured by a drop in capacitance value (Bergenthal and Prymak, 1995). Care was taken to select capacitor samples that were consistently oriented with the metallic layers horizontal to the board, as opposed to perpendicular to the board. These careful selection procedures were implemented to minimize variation in signals caused by process-induced manufacturing variation, including orientation and solder fillet size. Minimizing all other process-induced variation in the samples ensures that the changes in vibration response signals can be attributed to cracks created through flex-testing, providing a good control sample for optimizing the testing system and the techniques.

9.2 Setup and Data Collection

The test conditions for each set of MLCC samples were meant to be the same, however, changes to the system setup between the availability of the samples made for

minor variations in system configuration. Specifically, the motion stage, excitation laser and the fiber delivery system were replaced. However, the energy density and spot size on the surface of the capacitors were kept constant for all of the capacitor sample sets.

9.2.1 0805 Rectangular Cross-Section MLCC Experimental Setup

The inspection system was set up to measure the specimens as shown in Figure 9-2, where a top view of the capacitor on the board shows the positioning and relative size of the excitation and measurement laser spots. The entire device is only 0.080"x0.050" (2.03 mm x 1.27 mm), so the excitation spot nearly covers the open area on the surface. The infrared excitation laser and the He:Ne interferometer laser spots are coincident on the surface, and centered on the capacitor. The end termination layer and solder obscured the ends of the specimen.

9.2.2 0805 and 0603 Square Cross-Section MLCC Experimental Setup

In order to take a measurement, the inspection system was aligned to the capacitor as shown in Figure 9-2, where a top view of the capacitor on the board shows the positioning and relative size of the two laser spots. The entire 0805 capacitor is only 0.080"x0.050" (2.03 mm x 1.27 mm), so the excitation spot covers most of the open area on the surface. For the 0603 capacitor, measuring 0.060”X0.036” (2.09 mm x 0.78 mm), the minimum laser spot diameter fills the top surface of the capacitor. The infrared excitation laser and the He:Ne interferometer laser spots are coincident on the surface, and centered on the capacitor. The end termination and the solder obscure both ends of the specimen, but the infrared laser irradiates only the ceramic surface.

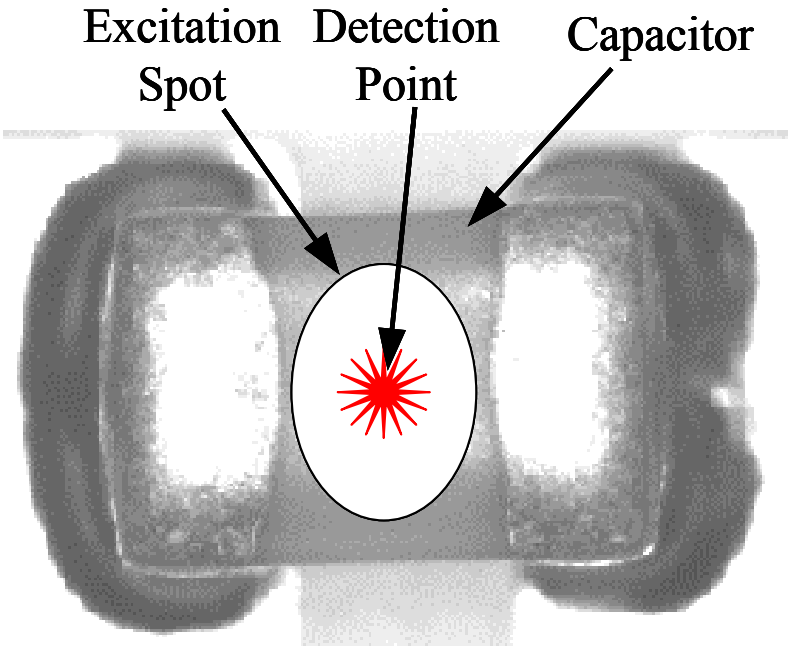


Figure 9-2: Experimental Setup

9.3 0805 Rectangular Cross-Section Results

Using the experimental procedure described, a vibration response was recorded from each of the 20 capacitors in the test batch. A first look at the recorded waveforms showed that one of them was extraordinarily different than the others, as shown in Figure 9-3. The magnitude and duration of the signal are much less than the reference device. On closer inspection, the capacitor was mounted on its thin edge. Since it does not have a square cross-section, the device was much stiffer in bending than the other devices. Unfortunately, this capacitor was one of the reference capacitors, so there are only nine reference waveforms that are valid.

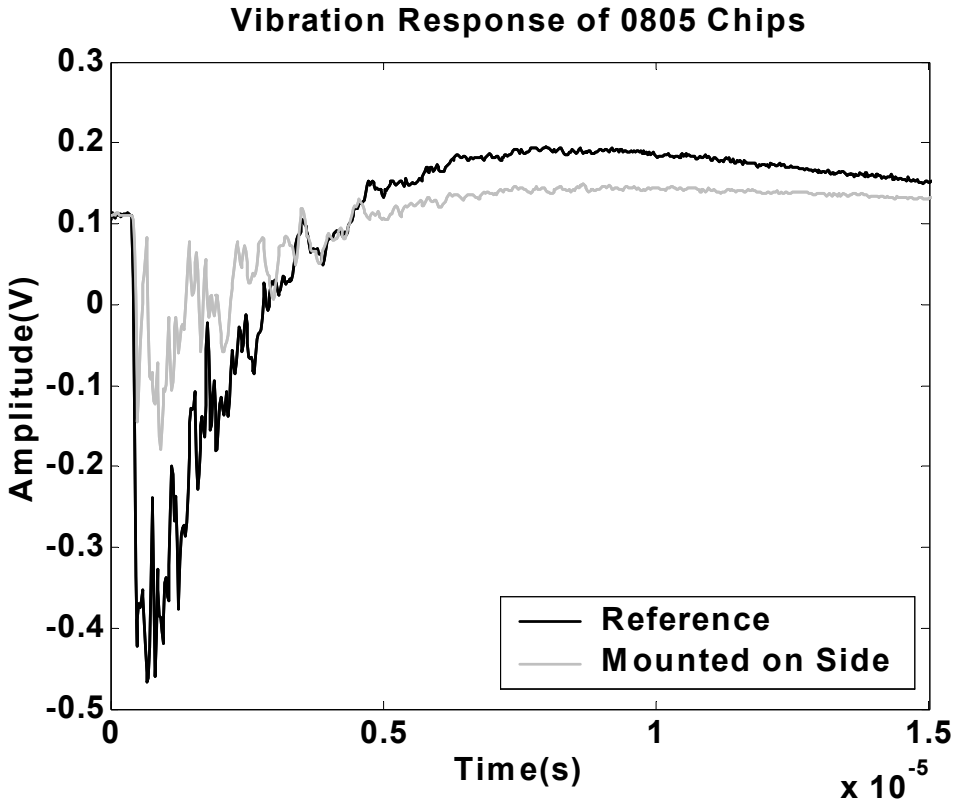


Figure 9-3: Time-domain Vibration Response for Capacitor Mounted on Side.

A more typical time-domain signal is presented in Figure 9-4 for both a flex tested and an as-manufactured device, and the large-amplitude, low-frequency displacement from the thermal heating is very evident because the laser spots are coincident. The minor vibrations are the modal vibrations that are of most interest for detecting defects because they are most likely to be affected by changes in the quality of the capacitor. These occur at much higher frequencies than the thermal displacement, and several modes are excited.

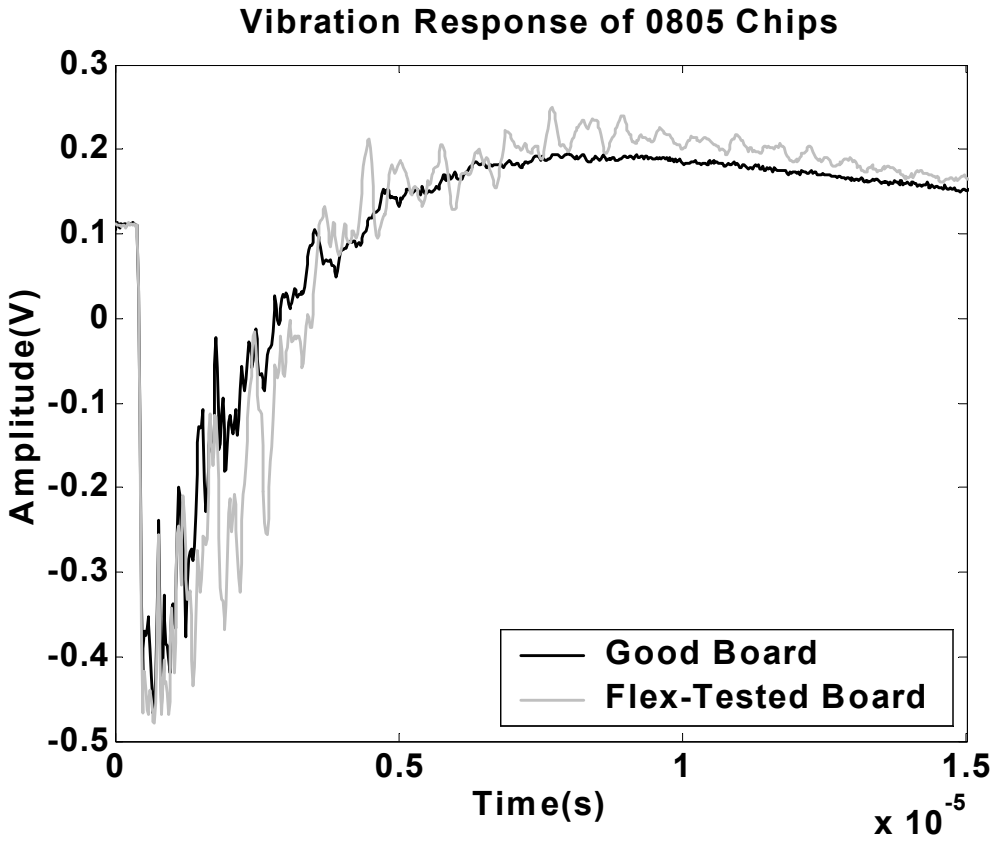


Figure 9-4: Time-domain Vibration Response for a Good and a Flex-Tested Capacitor.

The main difference between the good and the failed devices seems to be the magnitude and duration of the secondary vibration modes, as these modes have much larger amplitude in the devices that were flexed to failure. Cracking in the body of the chip decreases the stiffness of the system, and allows dissipation of the excitation energy through the various vibration modes of the capacitor.

9.3.1 Error Ratio Analysis

Because the magnitude of the vibration modes is difficult to measure directly, a signal analysis method has been previously developed for use with this system (Liu, *et.al.*,

2001). The Error Ratio (ER) has been discussed already in Chapter II and Chapter VI. The same algorithm is applied to the vibration response data from these specimens. Changes in size, material properties, or placement on a board may cause significant changes in the value, making this technique sensitive to all of these defects. Since the capacitors are much smaller than other device which have been tested, the acceptable manufacturing variation may cause a greater change in ER value than a defect.

Applying this method to compare the waveform from the chip mounted on its side to the rest of the chips yields the error ratio values shown in Figure 9-5. The error ratio values are calculated from the recorded waveforms, using the chip mounted on edge as a reference and comparing its waveform to waveforms from the reference capacitors and the flex-tested capacitors. A total of twenty values are shown, but the first value is identically zero because the waveform is compared to itself. The next nine values are from the reference capacitors, and the last ten are from those flex-tested to failure.

The values shown in Figure 9-5 highlight the effect of choosing an inappropriate reference. Little or no difference is observed between the two classifications of capacitors, because none of the other capacitors have the same geometry as the reference capacitor, making for an equally poor comparison with the device mounted on edge. However, the poor comparison can be used to identify a capacitor that was mounted on edge. The change in geometry for these test samples is significant enough to cause a major change in the error ratio values. More testing will need to be performed in order to measure the effect of a capacitor on edge when it has a square cross-section. In that case,

only the changes in the composite material properties will be changing the vibration signal for an undamaged chip.

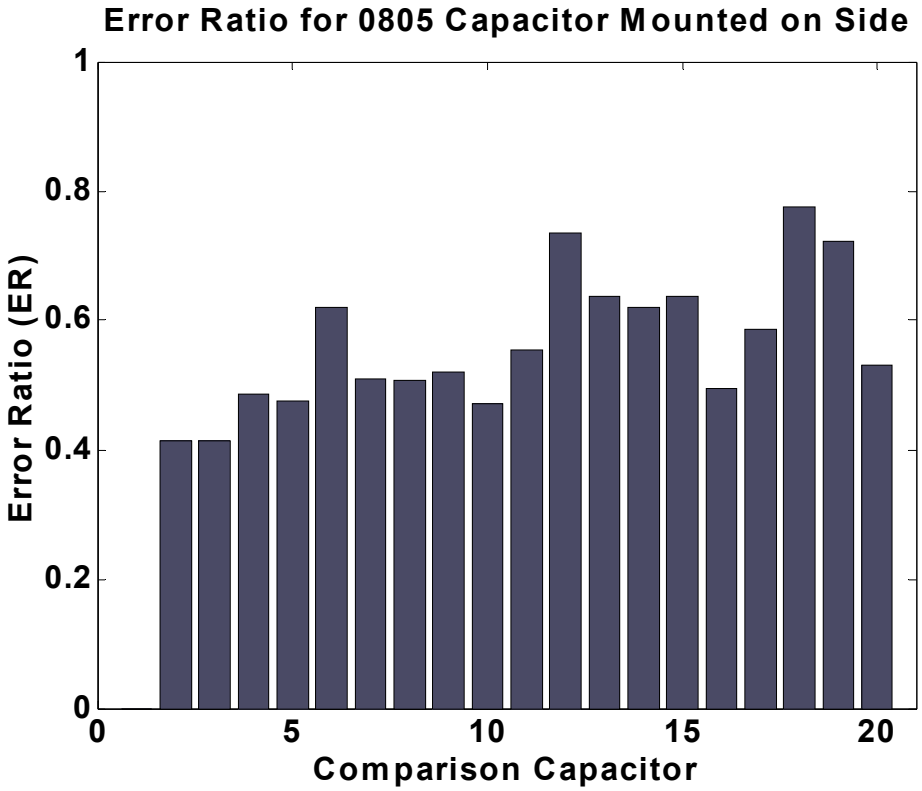


Figure 9-5: Error Ratio Values Compared with Capacitor Mounted on Edge.

Applying the error ratio algorithm to the rest of the data, using each of the reference capacitors in turn, provides a matrix of error ratio values which are presented in Figure 7, omitting the values involving the capacitor mounted on edge. Figure 9-6 shows the remaining nine reference capacitors along one axis, and the error ratio values calculated from comparing each of them with all 19 available waveforms, both reference

and flex-tested. The difference between the reference capacitors and the damaged capacitors is not very clear, so further signal analysis is necessary. The maximum values are about 0.01, which is an order of magnitude smaller than the values in Figure 9-5.

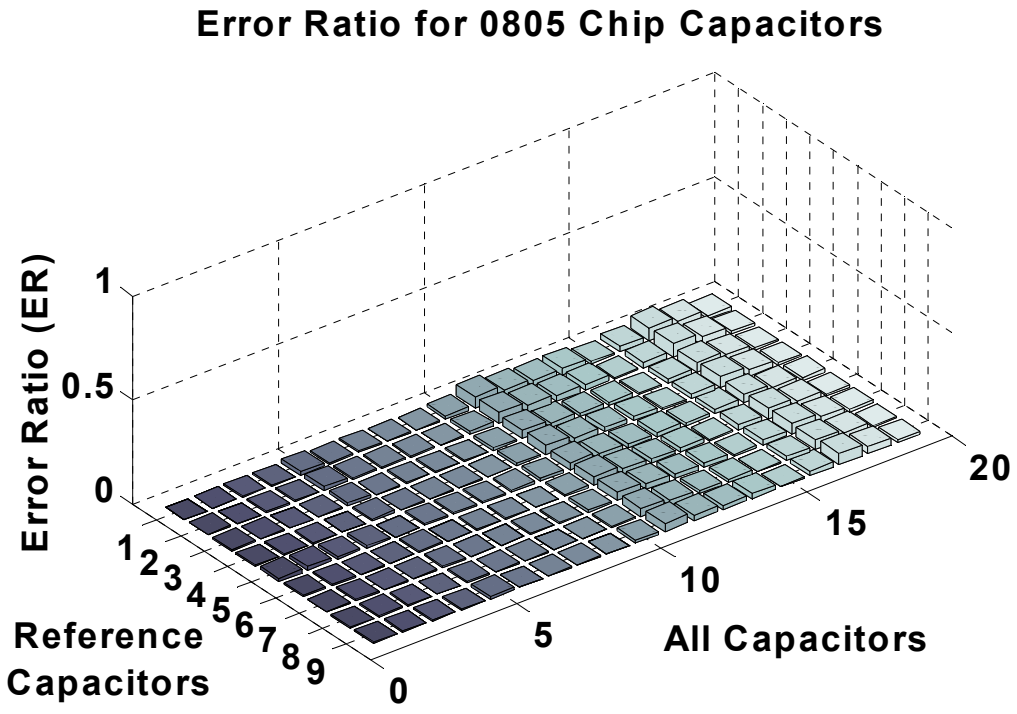


Figure 9-6: Error Ratio Distribution (Full Bandwidth).

To gain a better understanding of the content of the vibration signal, a fast Fourier transform (FFT) was taken of the waveforms plotted in Figure 9-4. The FFT plot, shown in Figure 9-7, reveals that specific vibration modes correlate with the flex-tested boards. Because the capacitor is excited with a broadband impulse from the infrared laser pulse, a broad spectrum of modes are excited. The first three vibration modes are identified,

based off the peaks on the FFT, and the power in each frequency range is much greater for the flex-tested boards.

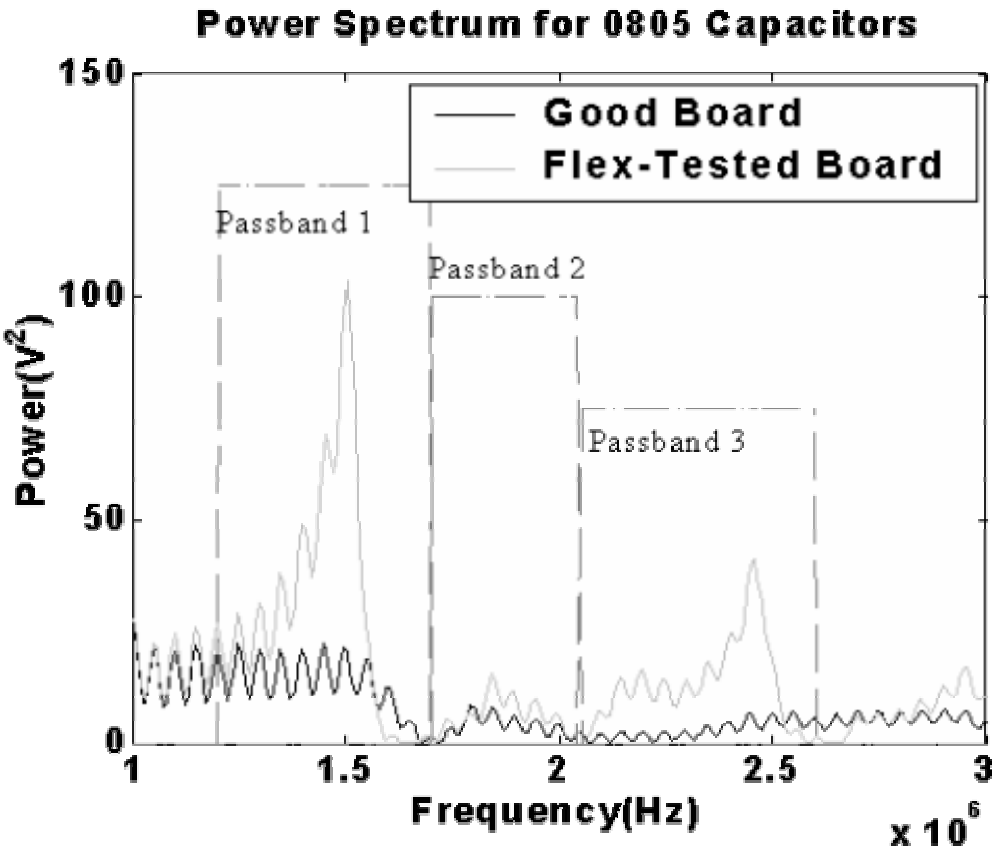


Figure 9-7: FFT of Full Bandwidth Signal with Passbands.

9.3.2 Vibration Mode Isolation Analysis

To isolate the effects of each mode on the time-domain signals and the error ratio values, three elliptical passband filters were designed and applied to the time-domain signals. The three filters have been centered over the first three observed modal vibration

frequencies of the capacitor being inspected, because these modes are stronger and more distinct than modes at higher frequencies. The ranges for the digital filters are 1.2-1.7 MHz, 1.7-2.1 MHz and 2.1-2.6 MHz, and they are labeled Filter 1, 2 and 3 in Figure 9-8. At the lower end of each filter there is some overlap with the other filters, but that was unavoidable with the close proximity of the vibration modes. Other vibration modes may be excited when the infrared laser pulses hit the capacitor, however, if the modes do not vibrate out-of-plane, they cannot be measured by the interferometer being used. The rest of the analysis shows the development and investigation of the error ratio values for each of the passbands and for combinations of the data from the passbands.

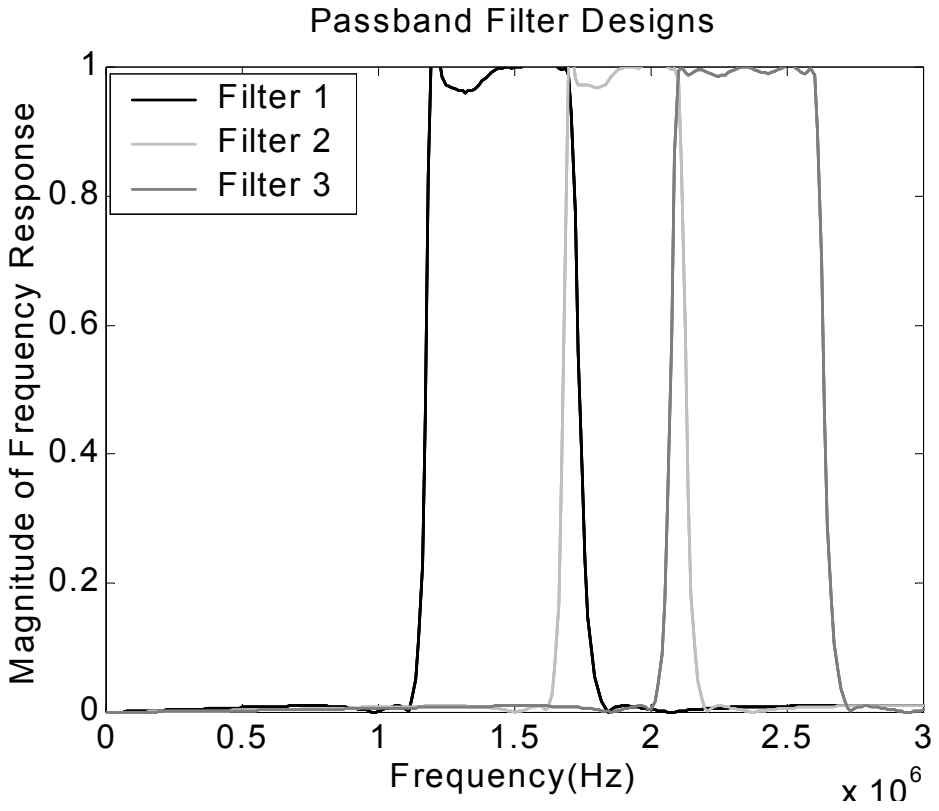


Figure 9-8: Passband Filter Designs for Three Capacitor Vibration Modes.

The time-domain signal of a damaged and a reference capacitor after the original signal was filtered through the first passband (1.2-1.7 MHz) are shown in Figure 9-9. The signal is very typical for a dissipative vibration response with more than one frequency. The increased power for the flex-tested board in the short bandwidth identified in Figure 9-7 appears as increased vibration amplitude in the time-domain, and the phase changes are caused by longer duration of specific frequencies. Using the filter makes the differences between the waveforms easier to view in the time-domain, so the total error ratio value calculated from this data will be much higher than the original value because the error ratio is scaled off of the normalized area under a reference curve. The large offset from the thermal response has been removed, so the change in the actual vibration signal contributing to the error ratio is proportionally larger.

The error ratio value matrices calculated from the data from the separate passbands are shown in Figures 9-10, 9-11, and 9-12. The layout is the same as Figure 9-6 with the reference capacitors along one side, and all of the capacitors, including the references, along the other side. The vertical scale for the error ratio values is the same as in Figure 9-6 to allow direct comparison between the frequency ranges and the original values. The only exception is Figure 9-12, where the vertical scale is much higher than all the rest because the error ratio values are larger.

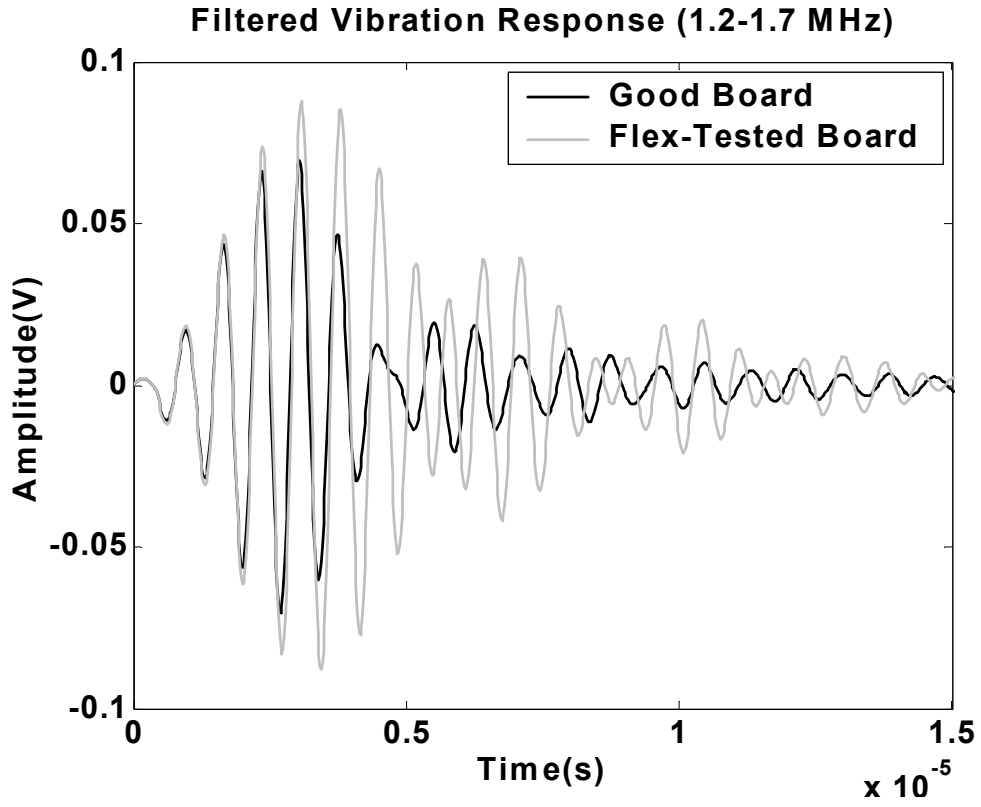


Figure 9-9: Filtered Time-Domain Signals.

The error ratio values presented in Figure 9-10 are calculated from the data created after applying the first passband filter. Compared with the original values in Figure 9-6, the error ratio values have been increased by almost an order of magnitude. The comparison of the reference values to each other shows little change between the entire set of reference waveforms, but the difference between the reference capacitors and flex-tested capacitors is very distinct, making identification of defective capacitors easy.

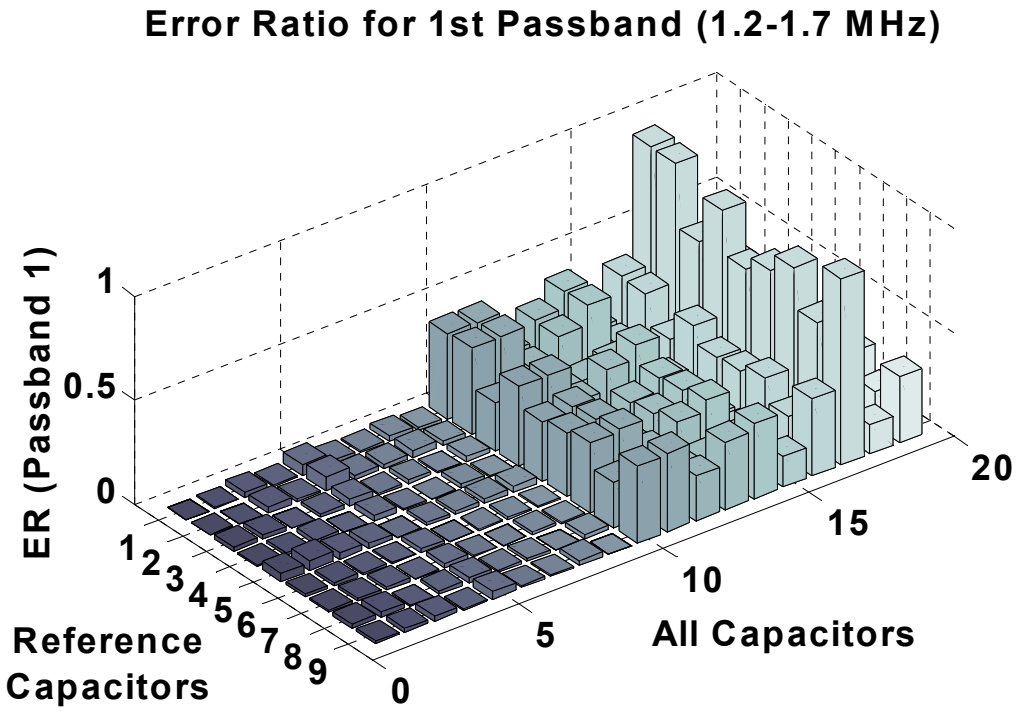


Figure 9-10: Error Ratio Distribution for First Passband (1.2-1.7 MHz).

Looking at the comparison of values for a single capacitor compared with all nine reference capacitors across the plot shows another improvement. The error ratio values are different for each measured capacitor, but similar when compared with all the reference capacitors. Because the trend is independent of the reference capacitor, the values are a clear indication that the vibration response has changed by a different amount for each of the flex-tested capacitors. These changes show a varying degree of damage for the flex-tested capacitors, and may correlate to different types, location or severity of defects.

Although the error ratio values from the first passband aid in differentiating the reference and flex-tested capacitors, the values from the second passband (1.7-2.1 MHz), shown in Figure 9-11, also differentiate the two groups fairly well. However, the data is more scattered, and the error ratio values calculated between the reference capacitors are much closer in value to the ones calculated for the flex-tested capacitors. Some of the comparisons between reference capacitors have error ratio values that are almost the same as the error ratio values for comparisons with the flex-tested capacitors. The data in this passband has a weaker correlation to flex crack defects than the first passband. However, it is still an acceptable indicator for current defects. Because each passband is centered on a vibration mode of the structure, other damage mechanisms may cause changes in this vibration mode that are more significant than the flex cracks.

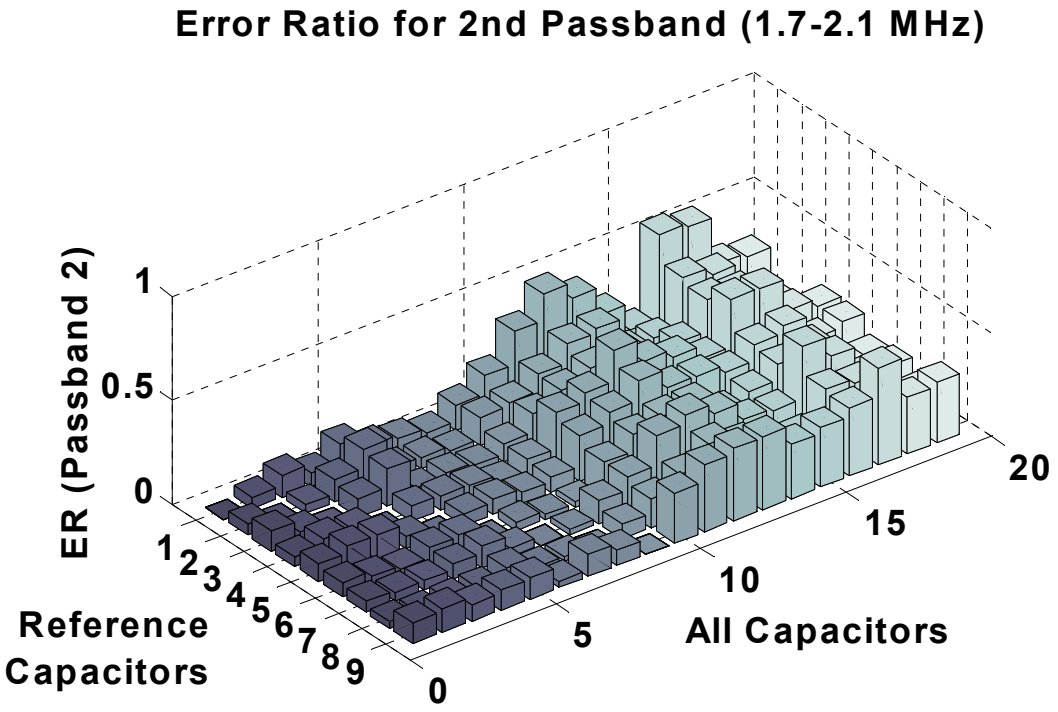


Figure 9-11: Error Ratio Distribution for Second Passband (1.7-2.1 MHz).

The third passband (2.1-2.6 MHz), shown in Figure 9-12, has the greatest impact on highlighting the difference between the reference capacitors and the flex-tested capacitors. With maximum error ratio values approaching 5.0, a sharp distinction exists between the flex-tested and reference capacitors. It is important to note that the vertical scale is five times larger on this plot than on the plots in Figures 9-10 and 9-11. The overall appearance of the data is much more consistent with the data in the first passband than the data in the second passband, with very consistent and constant values for the reference capacitors and a large increase in values for the flex-tested capacitors. The

greater range in the third band increases the resolution. Therefore, using this band in the future will help differentiate more subtle defects between capacitors.

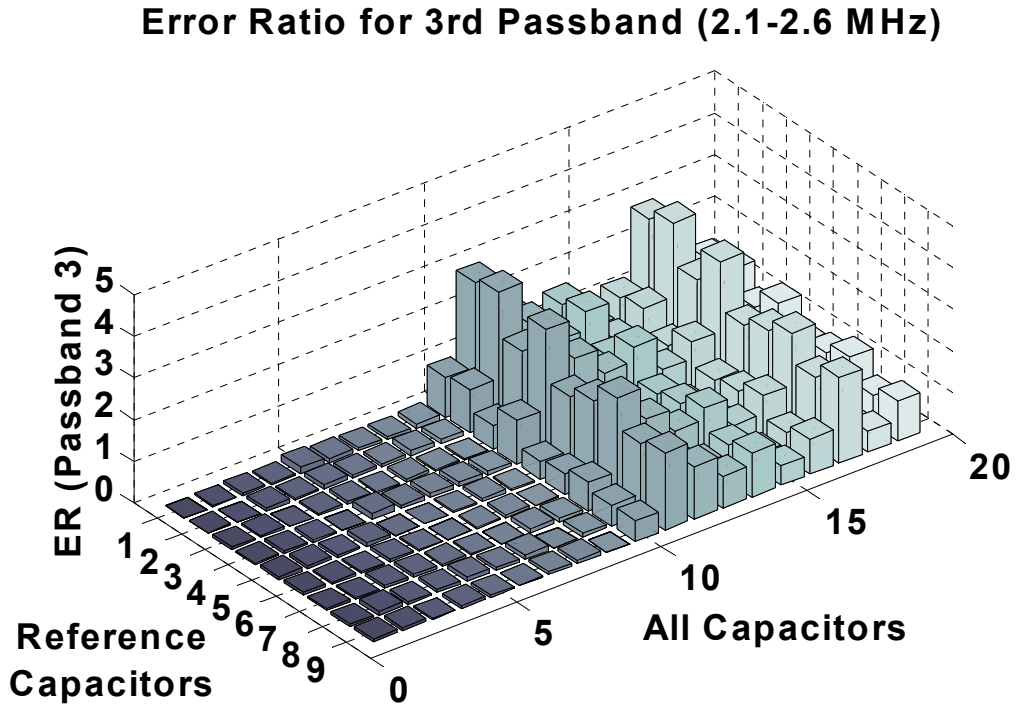


Figure 9-12: Error Ratio Distribution for Third Passband (2.1-2.6 MHz).

Increased range observed in the Error Ratio values in Figures 9-10, 9-11, and 9-12, show that the method of isolating a vibration mode in the time-domain has greater resolution than the full-bandwidth method used in previous work. Since the values are separated by a greater amount, incremental changes in overall quality can be more easily observed. Sensitivity differences between the three passbands are present, but they are difficult to explain, as they are modal vibration properties and are related to the geometry,

excitation method, measurement location, and defect location. Future analysis may correlate these changes to defect size, types, or location, but a larger sample set will be required.

The data collected from the 0805 MLCCs has shown sensitivity to the intentionally induced flex cracks. Although there were some changes in the time-domain vibration response waveforms between a reference and flex-tested device, the responses were too similar to identify a direct difference. Applying the error ratio calculation provides an effective way to quantify the differences between two vibration waveforms. Even though the values calculated from the vibration responses were initially small because the responses were overshadowed by the thermal displacement, application of the passband filters to isolate vibration modes drastically improved the signal quality used for the error ratio calculation. The vibration mode isolation approach is effective for increasing defect sensitivity to flex cracks in MLCCs when using the laser vibration technique. Therefore, this method is a viable option for online and offline quality assessment. The techniques presented have the potential to inspect these devices *in situ*, which is important for maintaining product quality in manufacturing.

9.4 0805 and 0603 Square Cross-Section MLCC Results

Using the experimental procedure described, a vibration response was recorded from each of the capacitors in both sample sets. Figure 9-13 shows a reference waveform from each of the two types of capacitors. The differences in the vibration response are from the change in geometry and the relative difference in energy density. The geometry change alters the natural vibration modes of the capacitors, and the relative change in

energy provides more amplitude of vibration. For both of the capacitors, a large, low frequency response dominates the time-domain response. The low frequency response is caused by the heating effect from the infrared laser excitation, and is recorded because the excitation and measurement points are coincident.

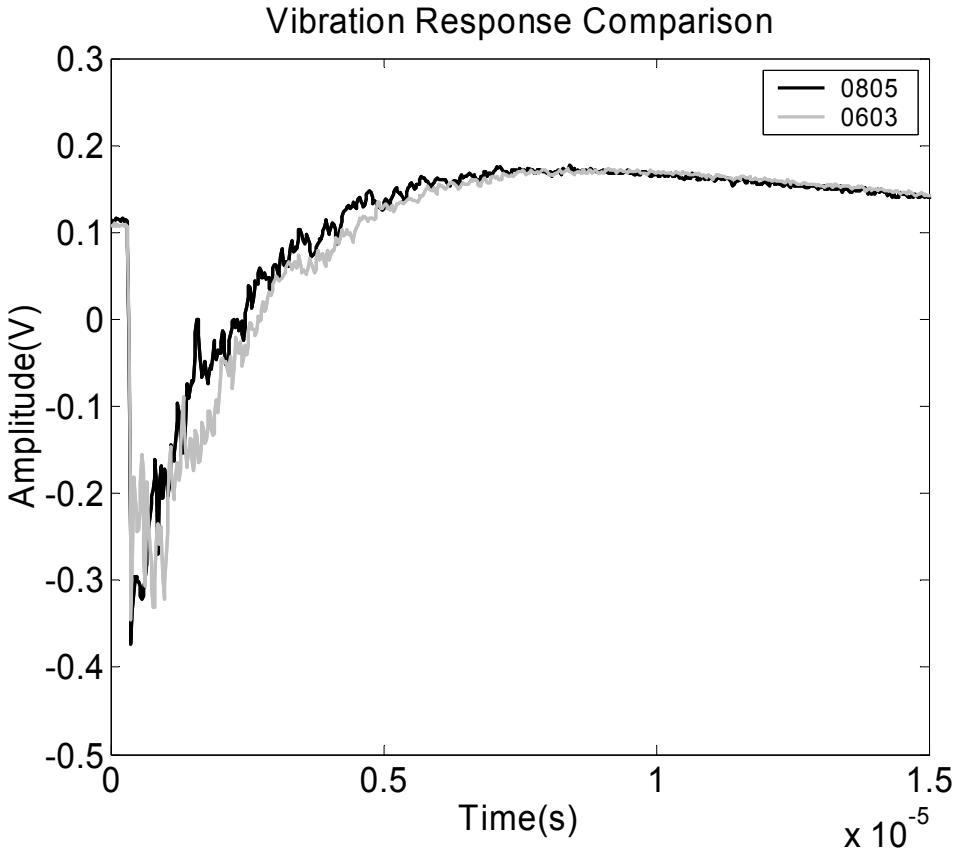


Figure 9-13: Vibration Response from the 0805 and 0603 Capacitors

The vibration responses of both as-manufactured (reference) and flexed-to-failure capacitors are presented in Figure 9-14. Although the signals have a similar overall response, dominated by the low frequency response related to the thermal effect of the

excitation laser, the differences between the signals, for a single size of MLCC, are in the high-frequency range. The high frequencies correspond to natural resonant frequencies (modal frequencies) of the capacitors. When a flex crack is present, the stiffness of the vibrating capacitor is changed, shifting the modal vibration characteristics to new values. Changes in the magnitude and duration of these secondary vibration modes are used to compare the vibration responses between the reference and flex-tested capacitors with greater sensitivity than using the full-bandwidth signal.

A fast Fourier transform (FFT) was performed on the data, and the resonant peaks are very prominent at frequencies above the thermal response, which has a broadband response below 1 MHz. Figure 9-15 shows the power spectra for both types of capacitor, highlighting the differences between a reference and flex-tested sample. For both the 0805 and 0603 specimens, several high-frequency resonant peaks are excited by the broadband laser impulse excitation. Some of these resonant vibrations are sensitive to flex cracks, while others are simply properties of the system. The challenge is to identify the frequencies that are most sensitive to defects and minimally sensitive to manufacturing or experimental errors.

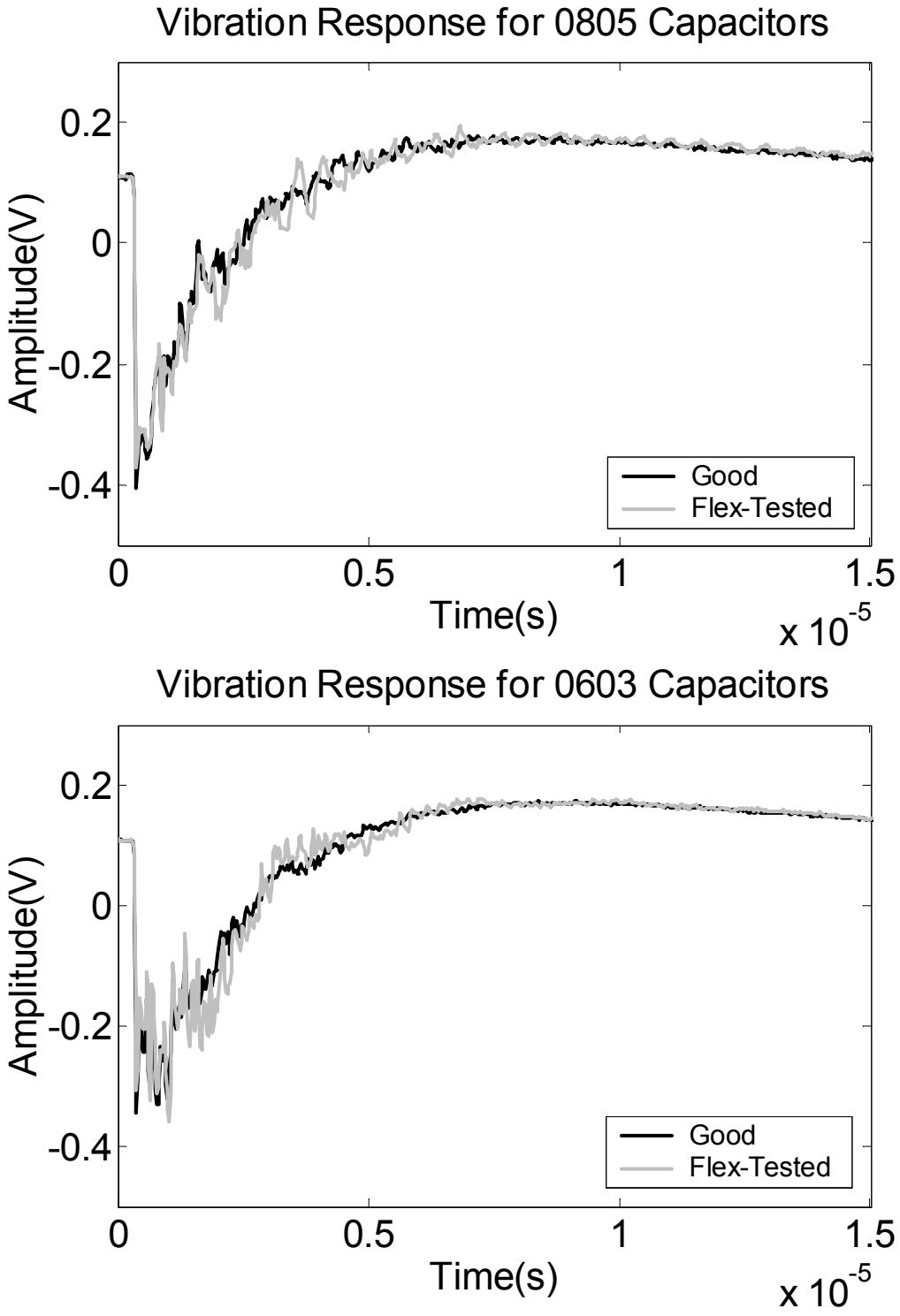


Figure 9-14: Vibration Response from As-Manufactured and Flexed-to-Failure Capacitors

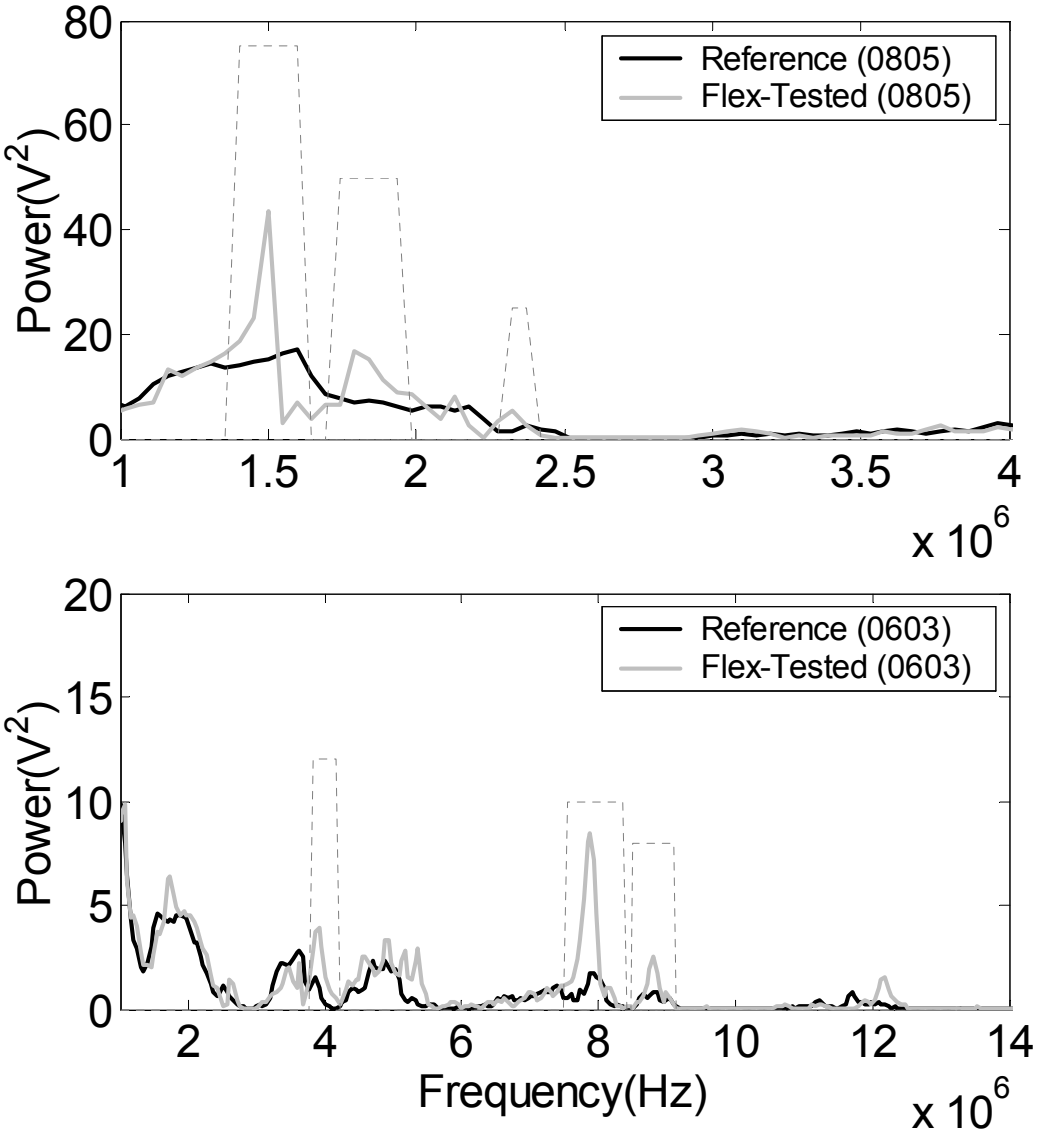


Figure 9-15: Power Spectra for 0805 and 0603 Capacitors

Shown in Figure 9-15, three passbands were selected for each device. Each of these passbands corresponds to a vibration resonant mode, and the time-domain data is filtered using elliptical bandpass filters to find changes in the vibration response for a single mode. Elliptic filters were chosen to provide a sharper cutoff frequency with less

ripple outside of the chosen band. Applying the filters provides an easy means of removing the thermal vibration component from the response, as well as minimizing the low-frequency environmental effects. Not all resonant peaks were selected. The selections were based off of stability between samples, and for showing a change in response to flex-testing damage.

9.4.1 Error Ratio Analysis

The Error Ratio method was applied to the data from the current set of MLCCs. Results are presented in the same format as the previous figures, so the data can be easily interpreted and compared with earlier results.

As another example of the ER method being applied to compare very similar signals, the three passbands identified for the 0603 capacitor are compared with their changing response to misalignment of the laser excitation spot on the surface of a sample capacitor in Figure 9-16. Two of the passbands are much more sensitive to changes in the location. The laser position was moved using the manual stage to misalign the spot across the small dimension in 100 μm increments both directions from the ideal central position.

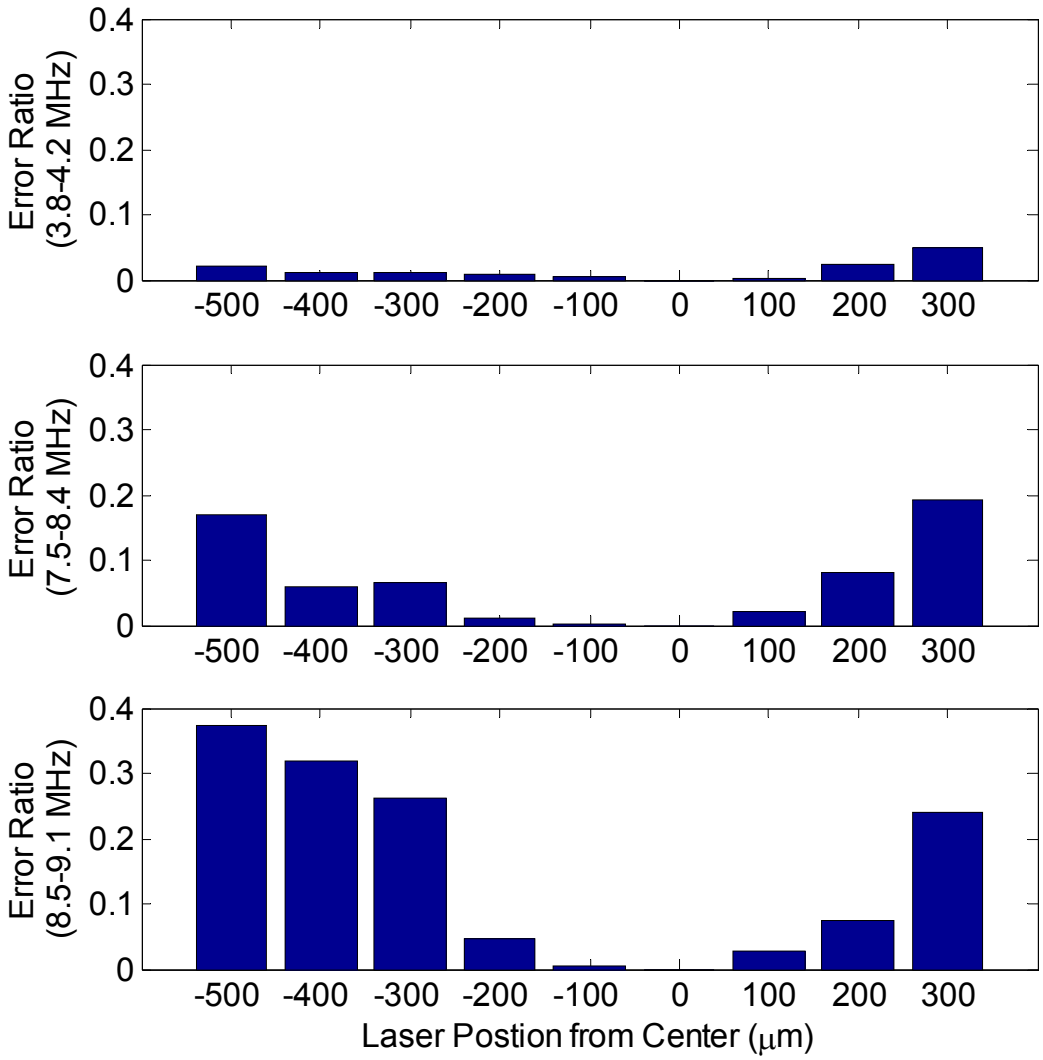


Figure 9-16: Laser Excitation Position Effect on 0603 Capacitor

The unequal changes in the Error Ratio values for each passband are easily explained. Resonant vibration modes are standing waves in the material, so misalignment can move the recorded vibration response from a node to an anti-node within the dimensions of the device. Lower frequencies have longer wavelengths, making them less susceptible to misalignment, but they can also be less sensitive to small

defects. However, the maximum alignment error for the system is much less than 100 μm, so this effect will not be a strong factor in the rest of the results. Figure 9-16 shows that a misalignment of more than 100 μm is needed before a large increase in Error Ratio occurs in the data.

9.4.2 0805 Capacitor Results

The Error Ratio (ER) algorithm, applied to the data recorded from nine reference 0805 capacitor samples and ten flex-tested 0805 capacitor samples, provides a matrix of Error Ratio values that are presented in Figure 9-17. Figure 9-17 shows the nine reference capacitors along one axis, and both the reference and flex-tested capacitors are shown on the other axis. The Error Ratio values calculated from comparing each reference capacitor vibration response with all 19 available vibration responses, after filtering with the first bandpass filter (1.4-1.5 MHz) to isolate the first vibration mode, are shown on the vertical axis. The difference between the reference capacitors and the damaged capacitors is clear, as the sharp increase in Error Ratio value indicates in row 10. The maximum value for all the comparisons between the reference capacitors is 0.034, and the minimum value from comparing all the flex-tested capacitors to the reference capacitors is 0.033. Therefore, the best and worst cases do overlap, however the average values from all the damaged capacitors are far above the average values for the reference devices.

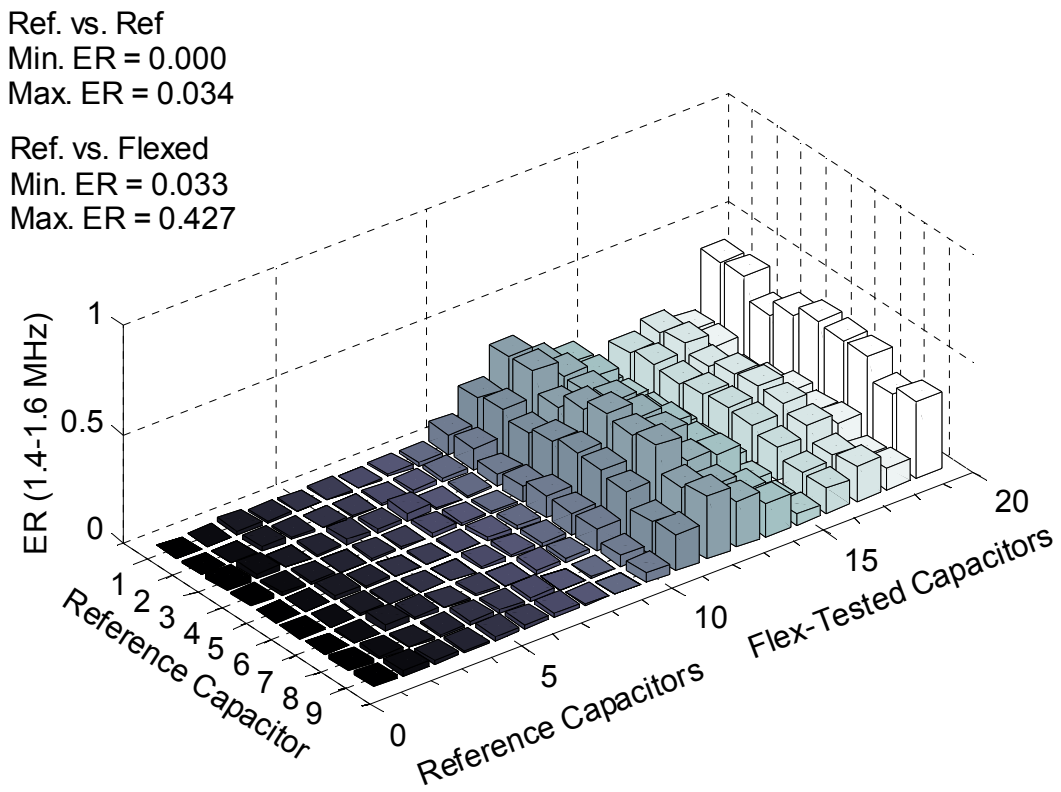


Figure 9-17: 0805 MLCC Passband 1 (1.4-1.5 MHz) Error Ratio Results

Figure 9-18 shows the same Error Ratio matrix, calculated for the second passband, 1.7-1.9MHz, and the results are better than the first passband. The maximum value for comparing two reference capacitors is 0.043, while the minimum value calculated from comparing the reference and flex-tested capacitors is 0.072. This is an increase of 30% between the two classes of capacitors, showing a strong correlation between the vibration response at this resonant peak (shown in Figure 9-15) and the flex crack damage. Values are consistent for all of the reference capacitors, so this mode is stable and sensitive to flex crack defects.

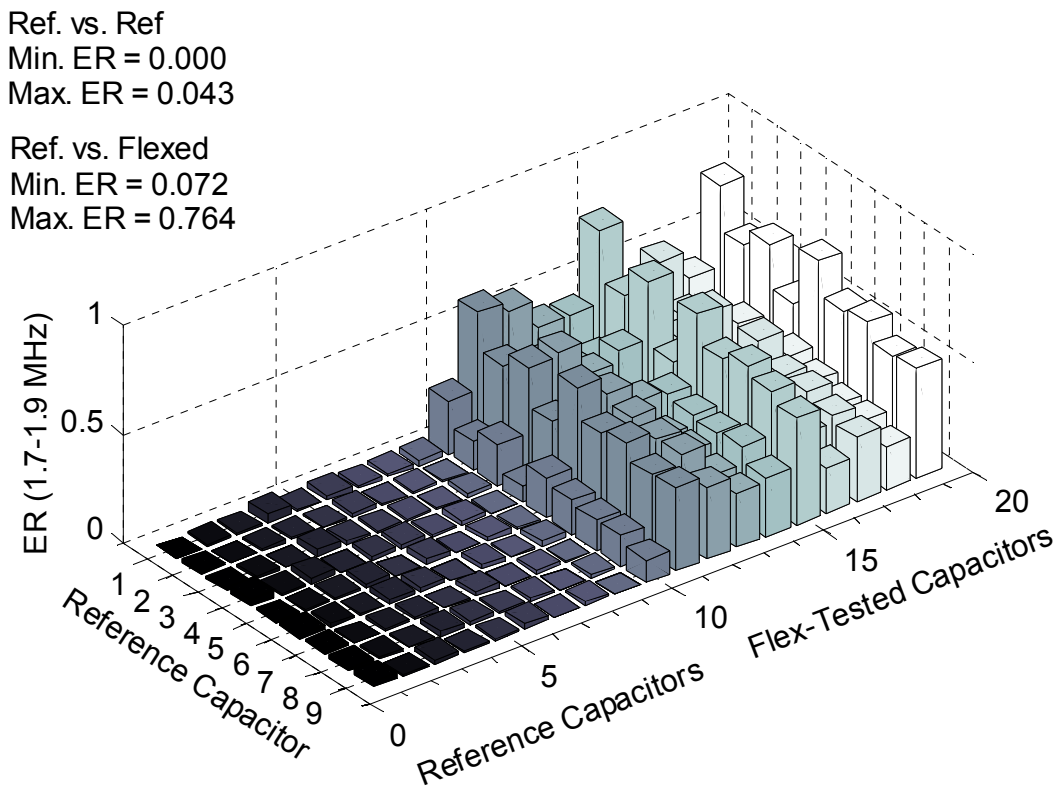


Figure 9-18: 0805 MLCC Passband 2 (1.7-1.9 MHz) Error Ratio Results

The third passband, 2.3-2.4 MHz, does not provide a clear delineation between the two classes of capacitors. The results, presented in Figure 9-19, are much noisier, indicating that this resonant mode is not as consistent as the first two. Part of the problem is that the maximum value of the peak on the FFT at the third selected resonant frequency is much less than the other resonant peaks, making detection of the vibration mode more difficult.

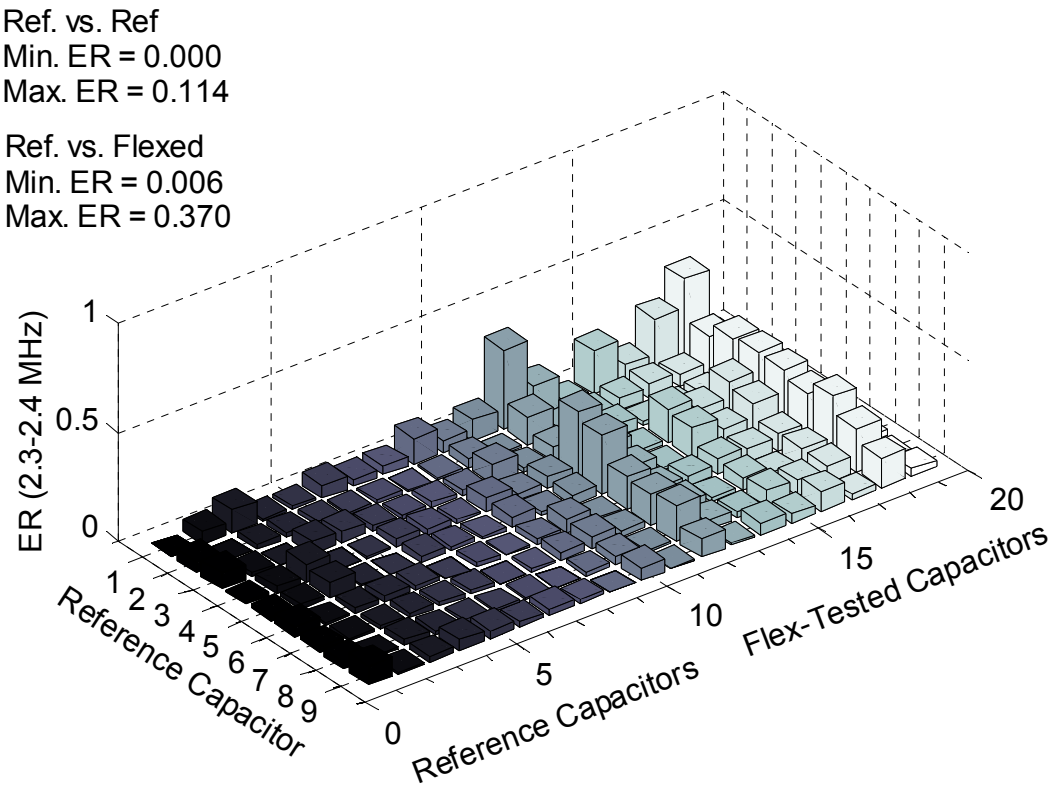


Figure 9-19: 0805 MLCC Passband 3 (2.3-2.4 MHz) Error Ratio Results

Even though the third passband is noisy, the first and second modes are adequate for providing a consistent level of discrimination. An expert system can be set up to combine the information from the two passbands, so that an Error Ratio value above an established threshold in either band will classify the capacitor as defective, and the part can be flagged for further testing.

One method of establishing a threshold is to average all the Error Ratio values calculated for a single capacitor, by comparing the vibration response from a single capacitor to the vibration response from all the reference capacitors. Figure 9-20 shows the average values for each capacitor, which shows the consistency of the vibration

inspection method. Passbands 1 and 2 show that a threshold can be established for classifying capacitors into good and flex-tested categories, because the nine reference capacitors have a much lower average value than the flex-tested capacitors. However, the average of the values in the third passband shows that it is still unsuitable for use as a discriminating value, even though some of the capacitors have a strong response at that frequency.

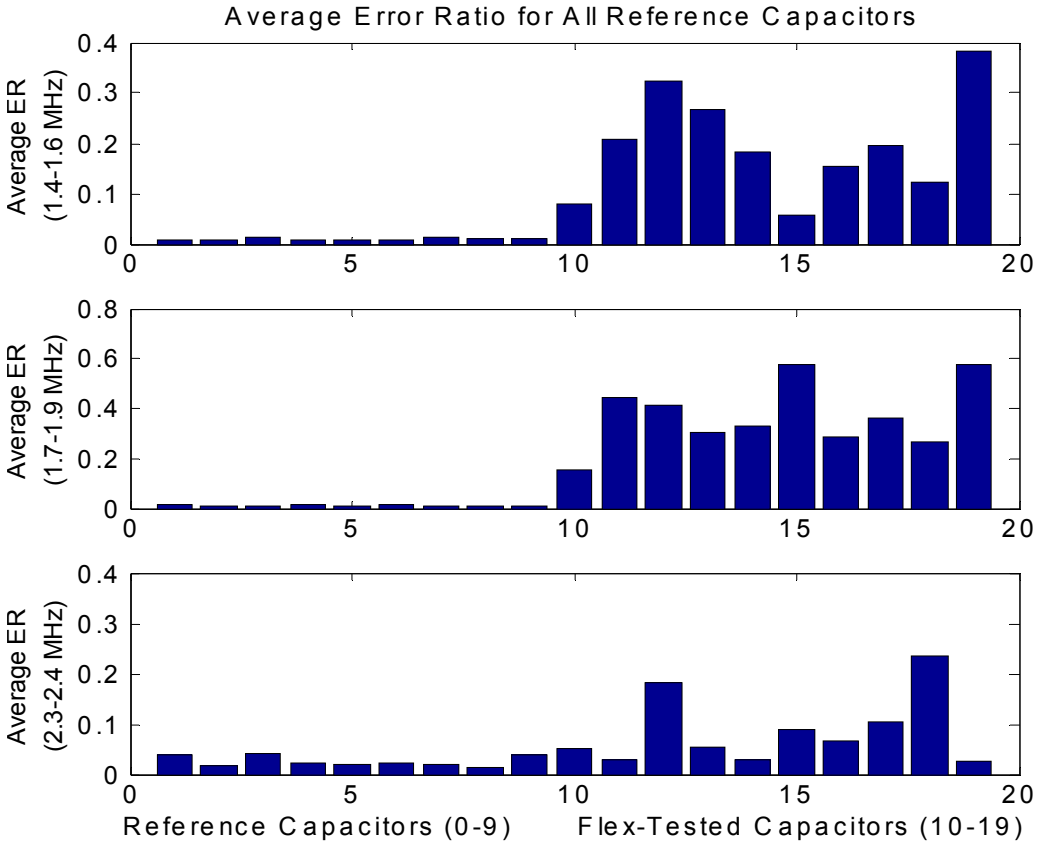


Figure 9-20: Average Error Ratio Values by Passband for 0805 MLCC

9.4.4 0603 Capacitor Results

The data from the 0603 capacitors was processed using the same Error Ratio algorithm, applied to the three passbands that were identified in Figure 9-15. Because the size of these capacitors is much smaller, the devices are considerably stiffer than the 0805 samples, which raises the natural resonant frequencies to a much higher numerical value. The first passband is 3.8-4.2 MHz, the second is 7.5-8.4 MHz, and the third is 8.5-9.1 MHz. As shown in Figure 9-7, not all of the resonant peaks were selected. The rejected resonant peaks were not consistently identified from the FFT of the vibration response for all of the sample capacitors, making them too unstable for use with the vibration analysis technique.

Vibration responses recorded from 10 reference capacitors and 15 flex-tested capacitors are compared, and the Error Ratio values for each passband are shown in Figures 9-21, 9-22, and 9-23. Figure 9-21 has the same layout as previous figures, and a sharp change is seen between the reference and flexed capacitors. However, the maximum value from comparing reference specimens is 0.76, while the minimum value from the flex-tested specimens is 0.051. A closer examination of the data shows that for each reference capacitor, the damaged capacitor has a greater Error Ratio value than the average of the reference capacitor comparisons.

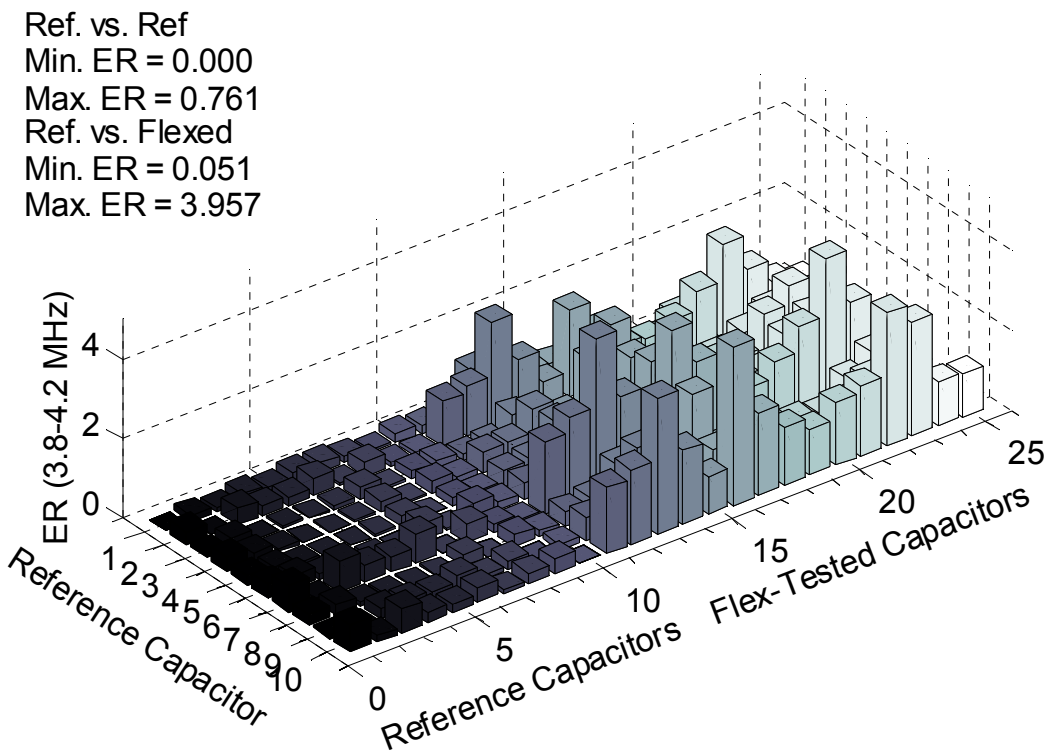


Figure 9-21: 0603 MLCC Passband 1 (3.8-4.2 MHz) Error Ratio Results

The results from the second passband are presented in Figure 9-22, and the results are similar to the first passband. Although a trend of high Error Ratio values separates the two groups of capacitors, occasionally, a low number is calculated for an Error Ratio value, making a direct classification difficult.

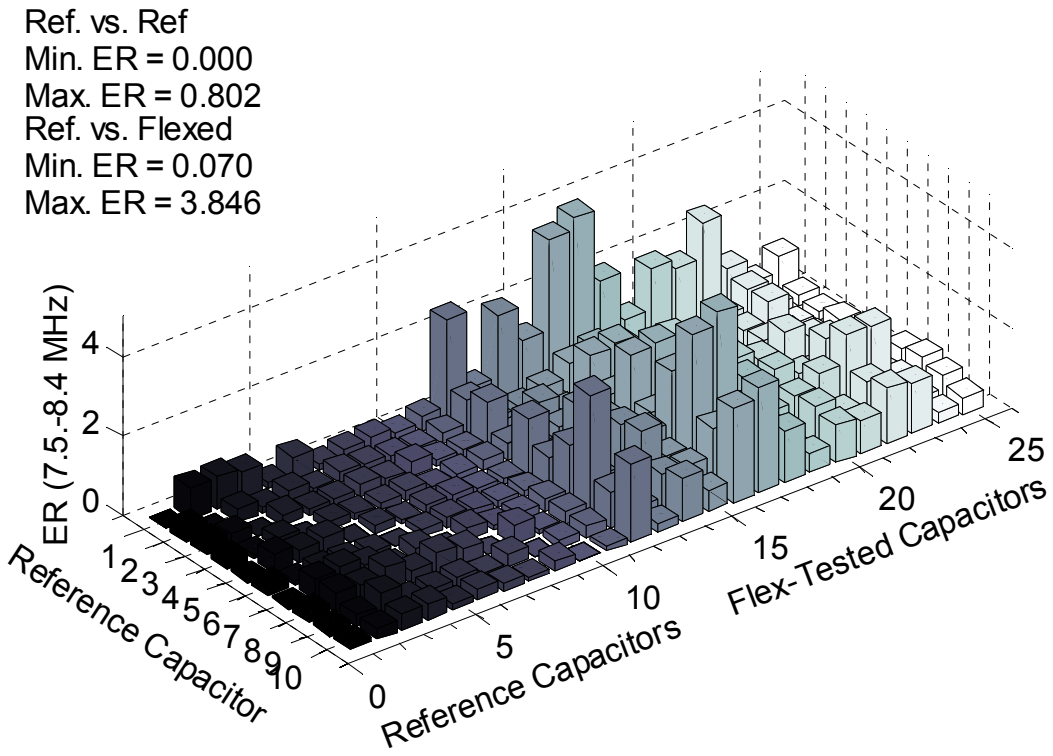


Figure 9-22: 0603 MLCC Passband 2 (7.5-8.4 MHz) Error Ratio Results

Results from the third passband, shown in Figure 9-23, are less useful than the results from the first two passbands. The erratic values and noise in the data can be attributed to the high frequency and the low power level of the resonant peak at this frequency range.

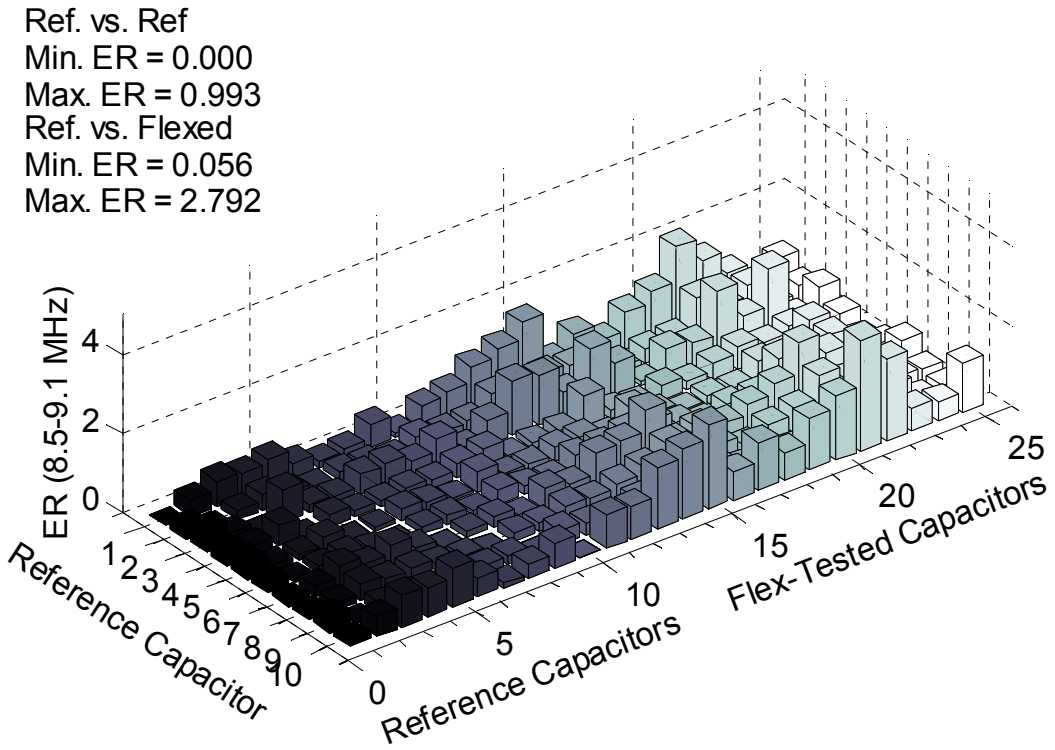


Figure 9-23: 0603 MLCC Passband 3 (8.5-9.1 MHz) Error Ratio Results

Figure 9-24 presents the average Error Ratio value calculated for each capacitor sample, by comparing the vibration response of the capacitor with the vibration response recorded for each one of the reference capacitors. Results are shown for each of the three passbands, and the distinction between the reference capacitors and the flex-tested capacitors is clear for passbands 1 and 2. However, the results from passband three remain too noisy to use. By averaging the values calculated using several reference capacitors, some of the manufacturing and measurement variability is removed. However, a clear threshold between the good and flex-tested capacitors cannot be established.

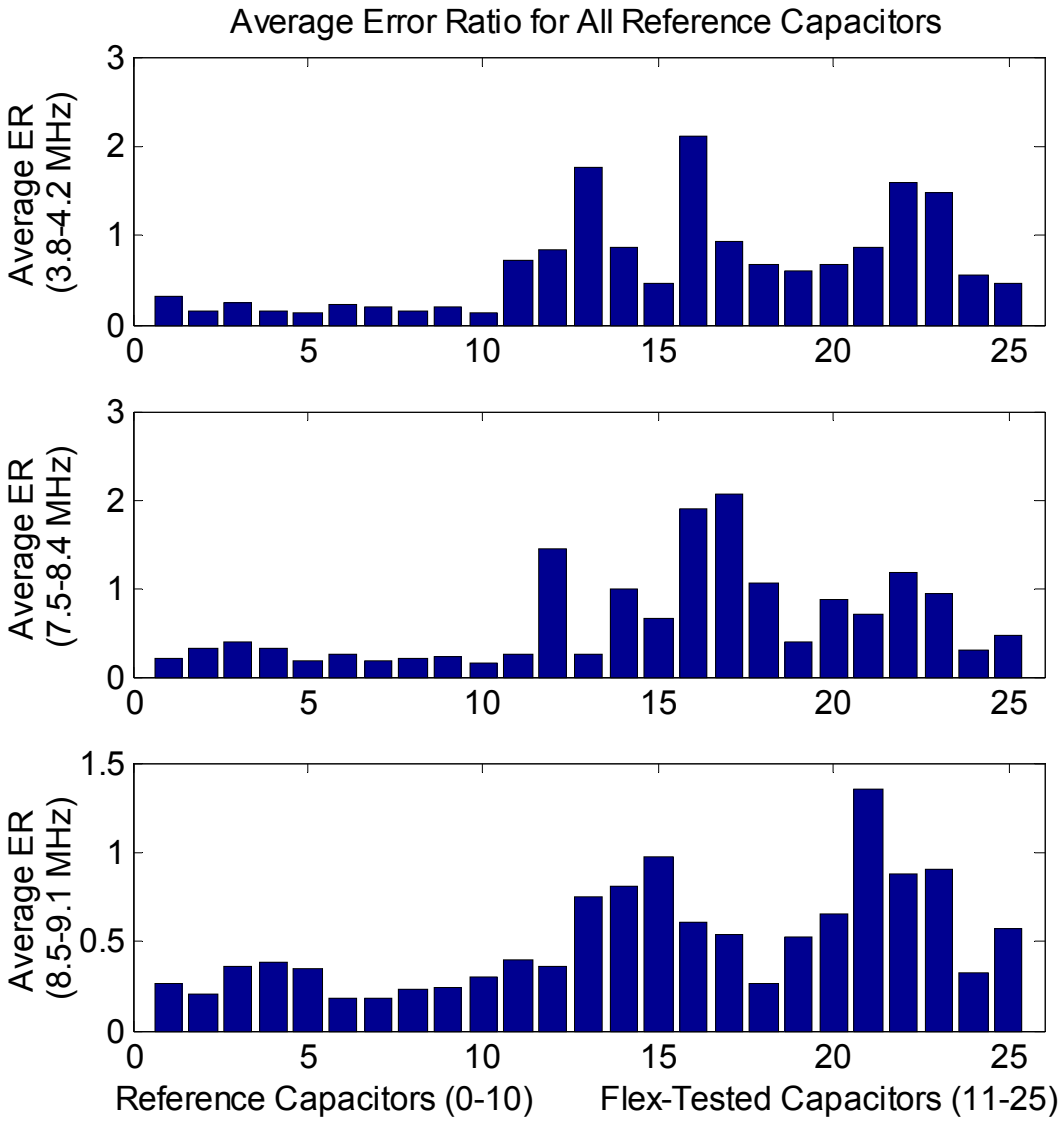


Figure 9-24: Average Error Ratio Values by Passband for 0603 MLCC

Because establishing a threshold value from the average Error Ratio values for each passband is not possible, an alternative method is used. In Figure 9-24, Capacitor 13 has a high value for passbands 1 and 3, but a very low value for passband 2, and other capacitors display a similar change in the Error Ratio value relative to the reference

values. To minimize the risk of missing a defective capacitor, the information from the three passbands needs to be combined to provide a total value for each capacitor. Therefore, the Error Ratio values from each of the three passbands are added together for each capacitor sample, compared with each reference. Then, the ten Error Ratio sum values are averaged to provide a single Error Ratio sum value for each capacitor sample, as presented in Figure 9-25. The ten reference capacitors have a maximum value of 0.996, while the minimum total of the flex-tested device is 1.16. Establishing a threshold is not hard using this method, and having a single number to base the discrimination between good and cracked capacitors makes automation more feasible.

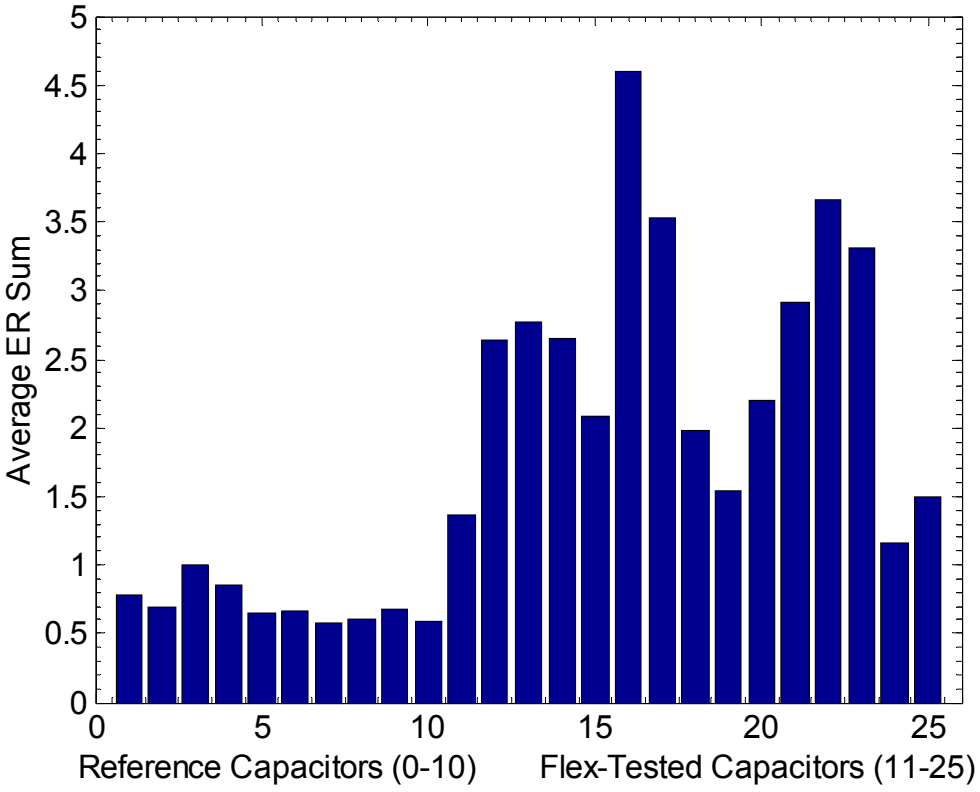


Figure 9-25: Average of Error Ratio Sum for 0603 MLCC

9.5 MLCC Conclusions

Although MLCCs remain a commonly used surface-mounted device, flex cracks caused by manufacturing processes continue to be a major failure mode. Previously, the laser ultrasonic and interferometric measurement system developed for microelectronic package quality assessment has proven to be useful in identifying flex cracks and MLCCs mounted on edge. Now, the technique has been validated on two additional MLCC capacitors with a square cross-section, and one of them is a smaller capacitor with a smaller cross-section. Since this technique is noncontact, nondestructive, low cost and fast, it has potential for use online as part of quality control procedures. The high accuracy achievable with more advanced signal processing makes this technique and system valuable for offline process optimization and error analysis. In addition, this inspection system has been used to find defects in solder bumped interconnections for flip chips and chip scale package (CSP) devices, so it can serve as a tool for inspecting multiple classes of surface mounted devices on one PWB (Howard, *et.al.*, 2003).

The system was able to detect the difference between reference capacitors and flex-tested capacitors using the previously established Error Ratio algorithm for laser vibration analysis. The current analysis technique uses passband digital filters, applied to the time-domain signals, to allow analysis of specific vibration modes with the Error Ratio algorithm. The algorithm compares a single-mode vibration response from a reference device to the single-mode vibration response from another device and computes a single-mode Error Ratio value. Since the Error Ratio values computed for a single vibration mode can be too noisy to identify cracked capacitors from good capacitors, the

Error Ratio values that were computed for each device in comparison with each of the reference devices were averaged to provide a single value. The average Error Ratio values show a clear distinction between the reference and flex-tested capacitors. Using the average Error Ratio values and a larger sample set, a threshold for capacitor quality can be established.

For this initial system development study, the capacitors and the boards were selected from single batches and processed at the same time, minimizing process-induced variation in the vibration response signals. Careful control over the samples ensured that the technique and the system were able to correlate changes in the vibration signal to intentionally-induced flex cracks. In the future, a correlation of changes in each vibration mode may allow identification of specific types of process-induced manufacturing defects, specific defect locations, or measurement of defect severity. However, in order to make this correlation, appropriate capacitors with failures created to represent incremental changes of the manufacturing process parameters that cause these failures will be required to enable calibration of the system. Similar capacitors will be required to determine the specific effects of other manufacturing variations, such as capacitor placement on the board, orientation of the metal layers, changes in size, and solder fillet size. Other manufacturing failures such as thermal shock cracks, open solder connections, or misplaced devices will also cause a change in the dynamic response, but these defects have not been detected, as samples containing these defects have not yet been identified.

Currently, 0805 and 0603 capacitors are two of the most common package sizes, however, many other common capacitors are smaller. Smaller sizes, such as 0402 and 0201, will become more common with decreasing package requirements. In order to continue to detect defects in these small capacitors, some experimental parameters will have to change. First, the excitation fiber will have to be smaller to have a spot that fits on the surface of the device. Additionally, the sampling rate will have to be higher as smaller devices will have higher vibration natural frequencies, as shown in the change between 0805 and 0603 capacitors. Finer control of stage and laser excitation position will be necessary to avoid errors caused by the excitation or measurement positions. All of these requirements are easily met with current technology.

To make the system more capable for online inspection, a neural network or refined expert system can be established to automatically classify the defects, as has been done for flip chips (Liu and Ume, 2003) (Liu and Ume, 2002). Several complications exist in an actual manufacturing environment: manufacturing variability in placement, capacitor size, solder fillet shape, and orientation of the internal layers of the capacitor. More extensive testing done online can lead to better parameters for classifying samples, and the neural network can learn the differences between devices and the tolerances that must be maintained. Overall, the vibration analysis technique is flexible and can be applied to the problem of detecting cracks in surface-mounted ceramic capacitors.

CHAPTER X

CONCLUSIONS

Laser-generated ultrasound has been used for detection of manufacturing defects in flip chips and multi-layer ceramic capacitors (MLCCs). With the completion of this research, this new approach for detecting defects is now applicable for flip chips, BGAs, chip scale packages (CSPs), and MLCCs. In conjunction with previous research, this inspection technique has been developed, tested and proven to be practical for detecting defects such as missing, misaligned, and open solder bumps. It can also be used for detection of mal-oriented, misaligned, cracked or chipped packages. Unlike other inspection methods, this technology has advantages such as being non-contact, non-destructive, and practical for on-line detection. The equipment and setup are lower in cost than automated x-ray or automated C-SAM systems, and it is sensitive enough to be used for process development and optimization.

The laser vibration method was used to excite modal vibration in flip chip components, as was presented by the surface mapping of the chips. Several modes were isolated, from 100 kHz to over 1MHz, making the effective range of the technique very broad. Repeatability and consistency data show that high frequencies are both more sensitive to changes in boundary conditions, but they are also more sensitive to manufacturing and measurement error.

Repeated trials on flip chips with intentionally created open bumps showed that the laser vibration system is extremely repeatable and that the technique is sensitive for measuring the presence of two or more open solder bumps under these chips. The changes in Error Ratio (ER) values is statistically significant when subjected to an ANOVA comparison. The presence of two adjacent open solder bumps is detectable in one trial, but the presence of one open solder bump requires more than one inspection.

Structural modal analysis methods were applied to the problem of flip chips with open solder bumps. Although natural frequency and damping ratio were not good indicators of the presence of open solder bumps, the mode shapes (eigenvectors) of individual chips provided a clear indication of the presence of defects. The method has approximately the same sensitivity as the ER method, but it is helpful in the developmental stage of research.

Finite element analysis confirms the modal behavior of the flip chip package. A full parametric model of the flip chip package was created using substructures for more accurate meshing. A modal vibration analysis was performed to extract the eigenvalues and eigenvectors from the FEA model. Material properties and part geometry values were found within published specifications after allowing an optimization routine to match the modal vibration solution to experimental results. After model optimization, the boundary conditions were changed to simulate the defects present in the experimental samples and the resulting structural modal properties matched the experimental trend. Defects can be detected through changes in the mode shapes, but changes in mode shapes are difficult to measure when only one open bump is present in the model.

Although the current work shows the difficulty in detecting one open solder bump, several opportunities for improvements in the procedure exist that may make detection of a single solder bump easier. Selection of samples from the middle of a large batch of commercial products would help alleviate assembly problems seen in small batch assemblies. A higher or lower laser power level could change the sensitivity of the vibration modes. Since the system is not completely automated, the possibility exists for operator to operator variation. The interferometer requires re-focusing at regular intervals, and an unfocused interferometer decreases the sensitivity of the system. Therefore, with some minor improvements the system has the potential to accomplish the goal of detecting one open solder bump.

The laser-ultrasonic technique was proven to be useful in detecting flex cracks in MLCC packages. By using passband isolation in conjunction with Error Ratio (ER) analysis, the presence of flex cracks was identified for three MLCC packages. An 0805 capacitor with a rectangular cross-section, an 0805 square cross-section capacitor and an 0603 square cross-section capacitor were validated using this technique, marking the first nondestructive means of evaluating this condition.

Signal processing techniques have been developed and tested to work in conjunction with these new samples, increasing the number of approaches that can be applied to future inspections. Passband isolation, working in combination with the ER values, can help reduce noise and the thermal effect in order to provide a clearer distinction between good and defective components. Modal analysis methods, focusing on the mode shape of the fundamental frequency, provide a more direct way to measure

the change in deformation of the structure. Both of these methods can be easily applied to future applications.

Although not all potential problems have been completely solved, this technique is extremely flexible. In addition, the technique is in it's infancy with room for improvement, while other techniques, such as x-ray and C-SAM, have reached maturity and their capability is already near the physical limitation of the technique. As electronic devices continue to decrease in size, the laser vibration technique may be the only technique that can follow the industrial need to inspect smaller and more complex electronic packages.

CHAPTER XI

SIGNIFICANT CONTRIBUTIONS

Although there are definite areas that can be more thoroughly developed, the progress made in the course of this project is very significant. This work shows the usefulness of laser-generated ultrasound as an inspection tool for detecting open solder bumps under flip chip packages and for detecting structural flex cracks in MLCC packages. The application of a fast, non-contact, non-destructive, flexible, and robust method for finding defects is a definite step forward for the electronics industry, aiding in the effort of increasing reliability.

The repeatability and sensitivity of the laser vibration technique was established for a flip chip package having open solder bumps. After performing multiple experiments to verify repeatability, consistency and safety to the chips, the error ratio method was shown to provide a clear distinction for chips with two more open solder bumps. Chips with one open solder bump can be separated from properly attached chips, if they are inspected more than one time.

Another contribution is the application of structural modal analysis techniques to electronics components. Although traditional methods, such as monitoring natural frequencies and damping ratios for changes, did not work well, changes in the

eigenvectors (mode shapes) did indicate the presence of open solder bumps. It was verified that the laser excitation did excite full-field modal vibrations in the flip chip packages, and vibration modes were identified as high as 1 MHz. As a result of the modal analysis work, a new research area can be explored which treats electronic components as small structures and subjects them to the same analytical procedures as bridges and skyscrapers. The modal analysis data also verifies the error ratio method for defect detection, as one of the basic assumptions was a modal vibration behavior.

Verification of the laser vibration method was achieved by creating and applying a parametric modal vibration model of an entire flip chip. The model parameters were optimized to match experimental data, and the resulting changes in vibration mode shapes matched experimental data. Application of this model to other flip chip packages will help direct future verification procedures for other flip chip packages.

For continuing the laser vibration research, the contribution of a method for creating intentionally defective samples was developed. Methods were developed for creating open solder bumps in flip chip packages and for creating flex cracks in MLCC packages. A consistent method for creating samples with known defects is essential for testing new inspection techniques.

CHAPTER XII

RECOMMENDATIONS AND FUTURE WORK

Although a lot of progress has been made toward the goal of vibration diagnostic analysis of surface mounted devices, current experimentation and analysis have suggested future directions in the research. Developments in hardware, software, and the modeling effort that will lead to a more thorough understanding of the problem are all possible at this point. The following sections detail a few of the potential development areas for this research effort.

12.1 Defective Specimens

One of the greatest challenges for completing research is the lack of available samples for testing. Before commencing testing on a new type of sample, clearly identified defects must be identified. Then, a method for creating these defects reliably and consistently without changing other parameters must be found. In conjunction with the creation of new specimens, more work can be undertaken to identify the manufacturing-related variations that are observed in the data. These artificially-induced defects must compare with real manufacturing-induced defects.

12.2 Sensors

The laser interferometer currently used for inspection is extremely sensitive, but small changes in surface roughness make the signal level (and signal to noise ratio) unstable. This is the primary roadblock to completely automating the system. Taking data point by point is also slow, especially since the devices that need testing are getting more complex. Therefore, an Electronic Speckle Pattern Interferometer (ESPI) system may be a viable option for full-field vibration measurements, making the primary limitation of the system the camera capture rate.

Alternatively, the interferometer could be replaced with a scanning laser vibrometer, allowing the capture of a single mode shape from a component surface. Although scanning laser vibrometers are not yet available with the capability to capture frequency components in the megahertz range, the fundamental natural vibration frequency of some electronic components, such as flip chips and BGAs, is about one tenth that value.

12.3 Excitation

Laser excitation is a great, non-contact method, however, it does limit the generation of ultrasound. To get more energy at higher frequencies, the laser power must be greater, the spot size must be smaller, and the damage threshold of the material must be higher. Therefore, to prevent damage to the chip, the laser excitation cannot be strong enough for every situation. Implementation of a laser array to increase power input over distributed spots or some other excitation method may be more appropriate.

Another alternative is to apply a multiple excitation scheme. By moving to a multiple excitation scheme, additional modes can be identified from the data, and inspection points will be closer to at least one of the exciation location, maximizing the potential for detecting a defect. Although the sensitivity of the current methods for detecting open solder bumps has limitations, an increase in the number of modes that are consistently excited should increase sensitivity of the technique for detecting open solder bumps.

Although laser-generated ultrasound provides a broadband source, a harmonic source may be a better means of determining modal vibration parameters. Therefore, base excitation with a piezoelectric driver may be enough to allow "tuning" of the vibration input to a resonant frequency, isolating the effect of one mode over all others. Then, a Bode plot of the system response to a single frequency input can be mapped for changes caused by damage. Alternative excitation methods, such as air jets, may not be able to achieve the high frequencies needed for the resonant frequencies seen in these packages.

12.4 Refinements on Current Approach

Because of the wide variety of surface-mounted and solder-bumped surface mounted components available, testing must be done to validate the inspection procedure for each one. Tests should be performed on Chip Scale Packages (CSPs), Ball Grid Arrays (BGAs), multi-chip modules (MCMs), chip resistors, multi-layer ceramic capacitors (MLCCs) and other new styles that are under development. As with any other technique, the future of this research will focus on how to increase the resolution to

maintain the ability to inspect smaller solder bumps in larger chips. In this work, the smallest defect detected is one open solder bump out of 48 bumps, however, some of the newer packages have as many as 1200 balls under one chip. The limiting factors will be inspection size and sensitivity of the laser interferometer, the ability of the infrared laser to properly excite the chip, and the ability to accurately position the instruments properly above the chip being inspected. Statistical analysis of vibration signal repeatability and the effect of acceptable manufacturing variation changes on the vibration signals will help define future sensitivity and detection levels.

To increase the ability of the system to detect smaller defects, advanced signal analysis methods must be used. In addition to the "Error Ratio" and FFT analysis, modal analysis, signal correlation and other measures of the changes in the vibration response of electronic components can be used. Although a neural network can be created, an expert system that focuses on specific parameters can be used to make the decision between a reference device and a defective component.

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